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Analysis and Chip Implementation of Clock Recovery For Coherent Satellite Communications

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코히어런트 위성통신용 클럭복원기의 해석과 칩의 구현

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ABSTRACT

In this paper, we suggest analysis and implementation of the single chip clock recovery for continuous and burst mode coherent satellite demodulations. Firstly, we describe the DPLL and its relationship to MAP phase estimation. Second description is linear analysis of recovery loop as a DPLL. The classically designed clock recovery circuits, which consist of several independent devices, are used to recover low speed data. We designed the chip to recover the clock whose data speed is maximum 200Kbps and to employ in the satellite demodulators using single chip clock recovery. The maximum system clock of the chip is about 20MHz. Its architecture shows complex implementation. Especially, The phase detector was designed the Lead/Lag Digital Phase Locked Loop(LL-DPLL) of nonuniform sampling schemes. This paper shows introduction of analysis and implementation scheme, design scheme, test results, and features of the chip.

要 約

본 논문은 연속 및 버어스트 모드 위성통신용 클럭복원기의 해석과 칩의 구현에 관한 것이다. DPLL과 그의 최대우도 위상검출기에 관한 해석을 설명하고 복원기 루프를 DPLL로서 선형 해석을 하였다. 전통적으로 설계된 클럭복원기 회로는 저속 데이타를 위한 클럭 복원 또는 독립된 다수의 부품에 의하여 구현되었다. 본 클럭복원기 칩은 위성통신 복조기에 사용하기 위하여 데이타 속도가 200Kbps이고 시스템 클럭이 20MHz까지 동작하고 그 이상의 속도는 적절한 외부의 위상 검출기의 도움으로 동작이 가능하도록 설계되었다. 본 칩은 게이트 어레이 기술에 의하여 설계되었으며 매우 압축된 구현 기법을 보인다. 특히, 비정규 샘플링에 의한 리이드/래그 DPLL로 설계되었다. 본 논문은 이의 해석과 구현 기법, 설계 기법, 칩의 특징 그리고 시험결과를 기술한다.

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Ⅰ. Introduction

The clock recovery represents the heart of the building blocks required in the implementation of coherent digital communications and tracking receivers. The continued progress in increasing performance, speed, reliability and the simultaneous reduction in size and cost of integrated circuits has resulted in strong interest in the implementation of the single chip clock recovery in the satellite communications. A digital version of the clock recovery alleviates some of the problems associated with its analog counterparts, difficulties encountered in building higher order loops, and the need for initial calibration and periodic adjustments. In addition, with the ability to perform elaborate real-time processing on the samples, the DPLL's can be made more flexible and versatile. In contrast to the study of the analog PLL, the development of all DPLL has just started to take shape over the last 20 years [1][2][3]. The earliest efforts on DPLL's concentrated on partially replacing the Analog Phase Locked Loop (APLL) components with digital ones [4][5]. The first all digital loop was reported by Drogin [6]. It was designed to track a relatively slow 30Hz sine wave. Different papers were published various aspects of implementation the DPLL concepts [7][8][9][10][11][12][13][14]. We have found several types of its implementations based on the scheme of phase detector. They are Flip-Flop DPLL, Nyquist Rate DPLL, Zero Crossing DPLL, and Lead Lag DPLL [10]. In this paper, we introduce single chip clock recovery which based on the LL-DPLL type phase detector. We describe the DPLL and its relationship to MAP phase estimation and linear analysis of recovery loop as a DPLL. Its resultant hardware is a first-order DPLL. The linear analysis consists of linear tracking in absence/present noise and sampling rate consideration. The clock recovery consists of four main functional modules, which are phase detector, digital filter, number controlled oscillator and alarm & test module. The chip will accept a TTL clock, up to 20MHz. The loop bandwidth of the digital transition tracking loop can be selected. Its design is very complex-reduction architectures using SOG 1.0 μm technology and the library of COMPASS vgt300039 base. This chip is intended for use in the Modems of satellite ground systems and digital radio systems. Its primary function is to adjust the frequency and the phase of a standard reference signal to produce a clock signal which is used to process the received data. The performance of this chip was tested using the real satellite Modem, which was embeded in the VSAT system via INTELSAT VII satellite links.

Ⅱ. Analysis of Clock Recovery Loop as a DPLL

1. The DPLL and Its Relationship to MAP Phase Estimation

The DPLL structure is the most easily motivated when one considers the problem of Maximum A Posteriori (MAP) estimation of a carrier with an unknown phase. Consider N discrete observables

$$y_k = s_k + n_k, \qquad 1 \le k \le N \tag{1}$$

where $\{s_k\}$ is a sequence of signal samples corrupted by the noise sequence $\{n_k\}$. The case of interest is

$$s_k = \sqrt{2P}\sin(\omega_0 t_k + \theta) \tag{2}$$

and represents the values of a sinusoidal sig-

nal observed at the increasing time epochs $\{t_k\}$. In (2), ω_0 is the known carrier frequency, P is the carrier power and theta θ is the unknown phase to be estimated. In order to proceed, we shall assume the noise samples are independant and identically distributed zero mean Gaussian random variables. Using Bayes' rule, the a posteriori Probability Density Function (PDF) of the unknown phase θ conditioned on the vector of observables $y = (y_1, \ldots, y_N)$ is given by

$$p(\theta|y) = \frac{p(y|\theta)p(\theta)}{p(y)} \tag{3}$$

In MAP estimation, one seeks to find a $\hat{\theta}$ so that the PDF $p(\theta|y)$ is maximized given the observables y. Using (3), this is equivalent to finding a $\hat{\theta}$ to maximize $p(y|\theta)\,p(\theta)$. To proceed, we shall assume that $p(\theta) = 1/2\pi, |\theta| \leq \pi$. Then, $\hat{\theta}$ also maximizes $p(y|\theta)$. By our assumption, $p(y|\theta)$ is Gaussianly distributed. Therefore, using the monotone property of the quadratic form

$$\Lambda(\theta) = -\sum_{k=1}^{N} \frac{1}{2}\left[y_k - \sqrt{2P}\sin(\omega_0 t_k + \theta)\right]^2 \tag{4}$$

Because $p(y|\theta)$ is a unimodel function, we know that $\hat{\theta}$ is the unique solution of

$$\frac{\partial}{\partial\theta}\Lambda(\theta)\Big|_{\theta=\hat{\theta}} = 0 \tag{5}$$

To continue, let

$$\Lambda_1(\theta) \triangleq \frac{\partial}{\partial\theta}\Lambda(\theta) = \sum_{k=1}^{N}\left[y_k - \sqrt{2P}\sin(\omega_0 t_k + \theta)\right] \cdot \sqrt{2P}\cos(\omega_0 t_k + \theta) \tag{6}$$

Equation (6) can be solved by the technique of simple iteration. In essence, given an abitrary starting phase estimate and provided some regularity conditions are satisfied, the equation

$$\hat{\theta}_{(l+1)} = \hat{\theta}_l + \Lambda_1(\hat{\theta}_l) \tag{7}$$

defines a sequence of $\hat{\theta}_l$ which converges to the MAP phase estimate $\hat{\theta}$. Equation (6) and (7) can be represented by the closed loop block diagram of Fig.1. For $\theta \neq \hat{\theta}$, the simplified equation is

$$\Lambda_1(\hat{\theta}) \cong \sum_{k=1}^{N} y_k\sqrt{2P}\cos(\omega_0 t_k + \hat{\theta}) \tag{8}$$

The resultant hardware scheme is the first-order DPLL [10]. The block diagram consists of two loops, $\sqrt{2P}\sin(\omega_0 t_k + \theta)$ and $\sqrt{2P}\cos(\omega_0 t_k + \theta)$, in Fig.1. The result in the equation (8) is the simplified form of the equation (6).

2. Linear Analysis of DPLL

In this section, we consider linear analysis of the digital transition tracking loop with first-order DPLL which represented in the equation (8). Due to the discrete nature of a DPLL, its operation must be described by dif-

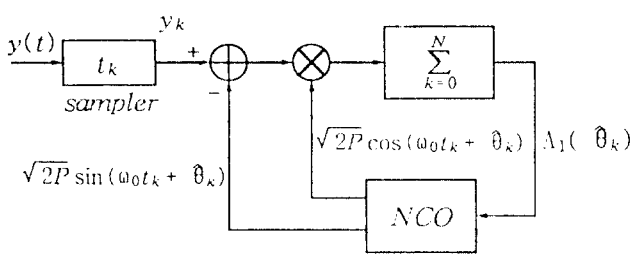

Fig. 1. MAP phase estimator

ference equation. In this section, the z-transform technique is employed to analyze the tracking behavior of a DPLL. This analysis is not limited to a particular class of implementations; the various implementation techniques are refelected in the difference equations governing their behaviors. Under the tracking assumption, the phase error samples are small and the gerneral nonlinear difference equation can be approximated by a linear one which can be solved by the z-transform technique. Some words of caution: in order to interpret and apply the linear result in a meaningful way, one must verify judiciously whether the tracking assumption is violated in any way for a particular application. Otherwise, the z-transform technique is simply not applicable and the results obtained are at best questionable.

〈 Baseband Model 〉

The baseband model for the DPLL block diagram of the clock recovery given in Fig.2. Both the phase detector characteristic g(•) and the equivalent noise samples are dependent on the particular loop implementation. However, the loop filter and the Number Controlled Oscillator (NCO) represented by $D(z)$ and $z^{-1}/(1-z^{-1})$ are common among all implementations. We have used z^{-1} to denote the delay operator, i.e., $z^{-1}q_k = q_{k-1}$. As a compact notation for manipulating with sequences, we define the two-sided z-transform Z[•] of a sequence $\{q_k\}$ to be

$$Z[q_k] = \sum_{k=-\infty}^{\infty} q_k z^{-k} \tag{9}$$

and denote $Z\{q_k\}$ by $Q(z)$ [10][17]. With this notation, we can represent the equation of operation of a DPLL compactly in terms of its local phase estimate

$$\hat{\theta}(z) = \frac{D(z)}{z-1}\left\{ g[\Phi(z)] + \frac{N(z)}{\sqrt{2P}} \right\} \tag{10}$$

and phase error

$$\Phi(z) = \theta(z) - \frac{D(z)}{z-1}\left\{ g[\Phi(z)] + \frac{N(z)}{\sqrt{2P}} \right\} \tag{11}$$

where it is to be understood that $g[\Phi(z)]$ denotes $Z\{g(\Phi_k)\}$. In this section, we shall assume that the DPLL is in the tracking mode with a small phase error about a reference phase (which we assume to be zero without loss of generality). In this case, $g(\Phi_k) \cong g'(0)\Phi_k$. Furthermore, we assume that $g'(0)=1$ since we can lump the gain $g'(0)$ with the loop filter $F(z)$. Using this assumption, one arrives at the linear loop equation for the phase error

$$\Phi(z) = [1 - H(z)]\theta(z) - H(z)\frac{N(z)}{\sqrt{2P}} \tag{12}$$

where

$$H(z) = \frac{D(z)}{(z-1) + D(z)} .$$

The reference [19] describes a fully-digital implementation of the carrier recovery loop currently implemented analog form. The emphasis is placed on carrier recovery loops employing an active filter or a phase lag-and-lead passive filter. By assuming that $\tau_1 \gg T$ in the equation (11) of the reference [19], the integral changes to the summation. As a result, the following equation is obtained

$$\varphi_{k+1} = \varphi_k - \alpha - \beta \sum_{j\geq 0} -j\lambda\, \varepsilon_{k-j} \text{ [19].} \tag{13}$$

The Fig.2 of the reference represents delayer, T, as a digital loop form. In this paper, we consider in the equations, from the equation (9) to the equation (19), as a digital one.

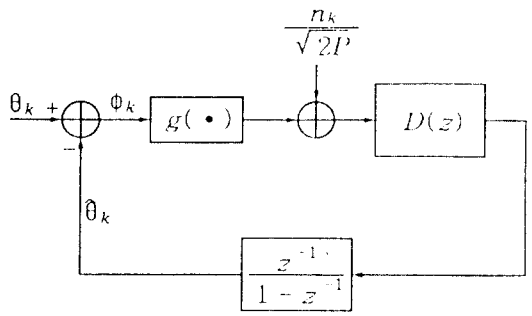

Fig. 2. The baseband model for clock recovery loop

〈Linear Tracking in the Absence of Noise〉

In the absence of noise, the phase error $\{\Phi_k\}$can be determined from the input phase samples $\{\theta_k\}$, from equation (12), namely,

$$\Phi(z) = [1 - H(z)]\theta(z) \tag{14}$$

using the inverse z-transform. In what follows, we shall concentrate on the special but important second-order loop,

$$D(z) = G_1 + \frac{G_2}{(1-z^{-1})}, \tag{15}$$

with the normalized parameters

$$1 - H(z) = \frac{(z-1)^2}{(z-\alpha)^2+\beta^2}. \tag{16}$$

The corresponding difference equation is

$$\Phi_k - 2\alpha\Phi_{k-1} + (\alpha^2+\beta^2)\Phi_{k-2} = \theta_k - 2\theta_{k-1} + \theta_{k-2}, \quad k = 0, 1, \ldots \tag{17}$$

with initial conditions $\Phi_{-1} = \Phi_{-2} = 0$ if we assume the DPLL starts at time t=0 with zero initial states. The impulse response of a homogeneous difference equation is a sampled version of the corresponding differential equation. In particular, if we let

$$\alpha = e^{(-\zeta\omega_n T)}\cos(\omega_n T\sqrt{1-\zeta^2})$$
$$\beta = e^{(-\zeta\omega_n T)}\sin(\omega_n T\sqrt{1-\zeta^2}) \tag{18}$$

the filter $H(z)$ is equivalent to its analog counterpart

$$H(s) = \frac{2\zeta\bullet\omega_n\bullet s + \omega_n^2}{\zeta^2 + 2\zeta_n\bullet s + \omega_n^2} \tag{19}$$

with normalized natural frequency ω_n and damping ratio ζ [10][16][17]. For the example, sinusoidal phase modulation (PM),

$$\theta(t) = \Delta\theta \sin\omega_n t \tag{20}$$

and for sinusoidal frequency modulation (FM)

$$\theta(t) = \frac{\Delta\omega}{\omega_m}\cos\omega_m t \tag{21}$$

where $\Delta\theta$ denotes peak phase deviation, $\Delta\omega$ denotes the peak frequency deviation, and ω_m denotes the modulation frequency, the steady-state phase error response is simply the steady-state frequency response of the equetion (16). In particular, for FM

$$\Phi_k = |1 - H(\omega_m T)|\frac{\Delta\omega}{\omega_m}\cos(k\omega_m T + \psi) \tag{22}$$

where the gain $|1 - H(\omega_m T)|$ and the phase shift ψ are determined from

$$|1 - H(\omega_m T)|e^{j\psi} \equiv [1 - H(z)]_{z = e^{(j\omega_m T)}} \tag{23}$$

The behavior of the steady-state phase error response as a function of the normalized parameter ζ and $\frac{\omega_m}{\omega_n}$ can be plotted and considered as a performance criteria of the designed loop [10][11][17].

〈Linear Tracking in The Presence of Noise〉

If the noise samples $\{n_k\}$are stationary with mean zero the steady-state variance of $\{\Phi_k\}$is given by [10][18]

$$\sigma_\Phi^2 = \frac{1}{2\pi j}\oint_{|z|=1} H(z)H(z^{-1})z^{-1}\frac{R_n(z)}{2P}dz \tag{24}$$

where

$$\hat{R}_n(z) = Z\{E(n_l\ n^*_{l+k})\}$$

is the z-transform of the noise autocorrelation function. In many practical cases, we can model $\{n_k\}$ to be uncorrelated zero mean with variance $\sigma_n^2 = N_0 B_i$ (B_i is a bandwidth associated with the noise variance and is usually the bandwidth of the IF filter preceding the DPLL). The one-sided loop bandwidth B_L is conveniently defined to be

$$\frac{2B_L}{B_i} = \frac{1}{2\pi j}\oint H(z)H(z^{-1})z^{-1}dz \qquad (25)$$

This yields $\sigma_\phi^2 = N_0 B_L/P$ which is identical with the analog result [10][17]. The loop filter will be sequential random walk filter which shows in Fig.4. This implementation consists of dividers, M and N. In the implementation of this clock recovery loop, the designed loop filter have selectable B_i (in the equation (25)). The filter have mainly a 96 counter and two 64 counters. Its integration time adjusted by the control signal. A high level on this inputs sets integration time such that digital filter require 32 data transition to produce an output. A low level produce an output every 8th data transition. Another control signal selects the divide ratio of the number controlled oscillator. its high/low level sets divide ratio to be 60 and 120 respectively. This operation is to determine divide ratio of the DPLL.

〈Relationship of Linear DPLL to Linear APLL〉

If the DPLL is in the tracking mode and the phase error is small ($\sigma_\phi^2 \ll 1$) so that the linear approximation, it is reasonable to assume that

$$\theta_k = \theta(kT) \qquad (26)$$

where T is the nominal clock period [10]. In that case $H(z)$ can be interpreted as a continuous filter

$$H_c(\omega) = H(z)|_{z=\exp(j\omega T)} \qquad (27)$$

Furthemore, if $H(z)$ is designed primarily as a low-pass filter with a bandwidth $B_L \ll 1/T$, then the DPLL approximates an APLL for

$$z = 1 + j\omega T\ ,\ \text{for}\ \omega T \ll 1. \qquad (28)$$

3. The Concepts of Design

We shall consider the design and realization of the fundamental building blocks for the DPLL in this section. The fundamental blocks consist of phase detector, loop filter and digitally controlled oscillator.

〈Constructing Elements〉

1) Pahse Detector

There are four main classes of sampling phase detector. The flip-flop PD is the output the set-clear flip-flop is set to "1" when a positive zero-crossing in the input signal is detected. A positive zero-crossing from the local estimate waveform then resets or clears the "1" value. The PD output is thus a binary valued waveform with a duration of "1" proportional to the phase error between the input signal and the local estimate. This error signal is used to control or gate a counter counting pulses generated from a high rate clock. The high rate clock usually has a frequency equal to $2^M \cdot f_o$ where f_o is the incoming frequency and 2^M is the number of quantization levels for the phase error state. We can assume that the counter is zeroed and starts counting when the flip-flop output switches from "0" to "1" and stops counting when the flip-flop output siwtches from "1" to "0". At that point, the content of

the counter is the digital representation of phase error which is accurate to with in $\pm\frac{\pi}{2^M}$.

The Nyquist rate sampling PD is that the sampling rate of the analog-to-digital converter(ADC) is chosen to be high enough so that the input signal can be reconstructed according to the Nyquist sampling theorem. In practice the sampling frequency is approximately equal to the bandwidth of the bandpass filter proceding the ADC. The digital samples are then multiplied digitally with the local reference samples to produce the required phase error samples.

There are two types of zero-crossing PD's. The first type samples on the positive zero crossings. This type of PD appears to be the simplest to important among all DPLL's. the second type samples on every zero crossing.

The lead/lag sampling PD is characterized by the simple binary PD output indicating whether the local reference leads or lags input signal.

In Fig.1, the MAP phase estimator is a second-order loop. The resultant hardware scheme for clock recovery was showed in the equation (8), which is the first-order DPLL with the factor of A_1 ($\hat{\theta}$) and $\sqrt{2P}\cos(\omega_0 t_k + \hat{\theta})$. In this design, we use the lead/lag sampling PD for clock recovery. Espacially, we use sequential random walk filter as a loop filter, which require lead and lag signals from phase detector.

2) Digital Loop Filter

The digital equivalent of the analog integrating element such as a RC filter is a digital accumulator. For the LL-DPLL, a different class of digital filters called sequential filters are employed. Since the PD output is binary, the sequential filter is used to smooth out the fluctuations seen at the PD output. The name sequential filter implies that the output is not a linear function of a fixed number of inputs. Instead, the sequential filter observes the inputs for a variable duration of time and gives an output when a certain confidence limit on the input is established. This procedure is very similiar to the sequential threshold test in estimation theory. The loop filter and the number controlled oscillator represented by $D(z)$ and $\frac{z^{-1}}{1-z^{-1}}$ are common among implementations. In the implementations, we have used z^{-1} as a delay operator. We designed the filter $D(z)$ as a sequential random walk filter which can be select filtering bandwidth.

3) Digitally Controlled Oscillator

Digitally Controlled Oscillator (DCO) is basically a programmable divided by N circuit. Its functional block consists of comparator, counter, and stable oscillator. The output of a stable oscillator is used drive the counter which increased by one every clock cycle. The content of the counter is compared with the input and when they are matched the comparator puts out a pulse which serves to be DCO output and to reset the counter. By varying the control input N, the DCO period can be controlled. In this design, we consider DPLL of the equation $H(z)$ in the equation (12) using digital transition tracking loop which consists of phase detector, loop filter, loop selector, and number controlled oscillator.

〈Sampling Rate Consideration〉

The sampling rate 1/T is typically selected to minimize the loop tracking error due to thermal noise and input phase dynamics. Based on results from analysis of tracking in the absence and present noise, one can show

that the DPLL's noise bandwidth increases as the sampling rate decreases while holding a constant phase error for tracking dynamics like a frequency ramp. To avoid threshold degradation, the requirement is $B_LT \leq 0.1$. The equation (28) is also satisfied under this condition [10].

〈Hardware Considerations〉

The input signal in the total clock recovery circuit is sampled and compared with a reconstructed reference to produce digitized error samples which are proportional to their phase difference. These samples are filtered by digital sequential random walk filtering technique and the corresponding output samples are used to control the priod of the NCO. If the loop is designed properly, the reconstructed reference will be forced to resemble the input signal. Many type of DPLL's built and reported upon thus far have been designed for low-speed applications such as subcarrier demodulation [5][7][9][14]. One important reason implemented low-speed is logic speed limitations. For designing DCO, the performance for critical components, ECL logic prescalers, is 350MHz clock frequency. The performance for monolithic LSI is 40ns per combined operation for designing loop filter. One for combined DCO and loop filter is 8MHz clock. In this paper, we show enhancement of operation performance using schemes of complex-reduced design and implementation schemes of single chip by ASIC design process.

Ⅲ. Digital Clock Recovery Implementation Approaches

In this section, The design and realization of the fundamental blocks for DPLL which are the phase detector, the loop filter, and the number controlled oscillator. The Lead/Lag sampling Phase Detector (PD) shown in Fig.3 is characterized by the sample binary PD output indicating whether the local reference leads or lags the input singal. In many ways, this is similar to the positive zero-crossing PD with a binary quantized phase error output.

However, because of the harsh quantization used, a sequential filter is often used to

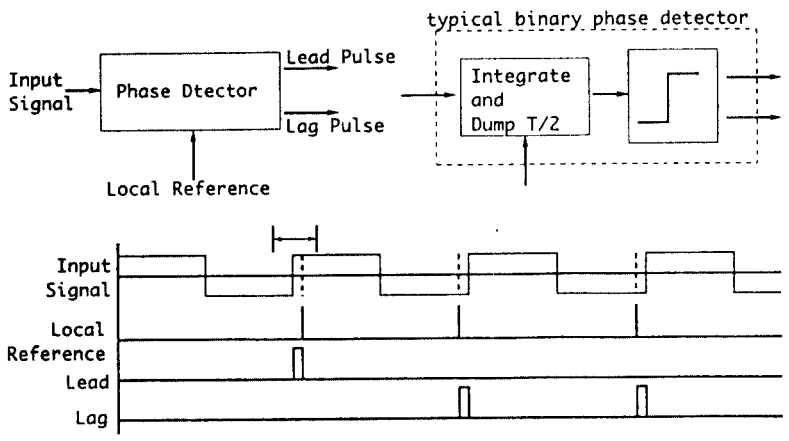

Fig. 3. The scheme of the Lead/Lag type phase detector

smooth the correction voltage applied to step the local number controlled oscillator. The digital equivalent of the analog integrating element such as a RC filter is a digital accumulator. It is simply designed using an adder and a unit delay connected. By employing two accumulators in tandem, one obtains a digital approximation to a double integrator. The construction extends obviously to higher order approximations. For the LL-DPLL, a different class of digital filters called sequential filters are employed. Since the PD output is binary, the sequential filter is used to smooth out the fluctuations seen at the PD output. The name sequential filter implies that the output is not a linear function of a fixed number of inputs. Instead, the sequential filter observes the inputs for a variable duration of time and gives an output when a certain confidence limit on the input is established. This procedure is very similar to the sequential threshold test in estimation theory. A representation sequential filter is depicted in Fig.4.

The N-before-M filter operates as follows. Lead and lag inputs are accumulated seperately in the N counters while both the lead and lag inputs are accumulated in the M counter. Assume initially that all three counters are reset. The random sequence of binary inputs continues untill one of two conditions is met: 1) If one of the N-counters in the figure fills up before or simultaneously with the M counter, then the corresponding output is produced, all three counters are reset, and the cycle begins anew. 2) If a total of M lead+lag inputs occurs before N inputs of either type, all registers are reset and no output is produced. The latter condition is most likely when the phase error is near zero. NCO is basically programmable divided by N circuit. The output of a stable oscillator is used to drive the counter which is increased by one every clock cycle. The content of the counter is compared with the input and when they are matched, the comparator puts out a pulse which serves to be the NCO output and to reset the counter. By varying the control input N, the NCO period can be controlled. In Fig.5, we show the LL-DPLL block diagram due to [15].

The sequential loop filter is suitably to estimate whether the local clock lags or leads the signal input. Other than that, the LL-DPLL is very similar to a ZC-DPLL with one-bit phase error resolution.

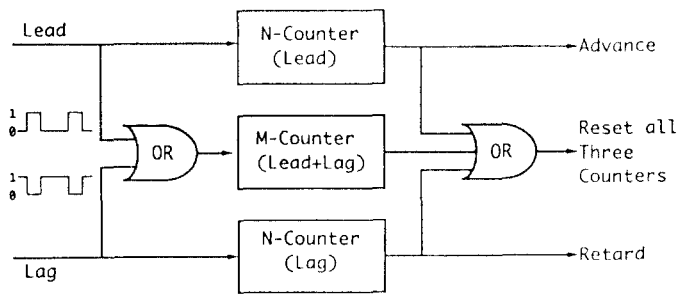

Fig. 4. The scheme of the digital sequential filter

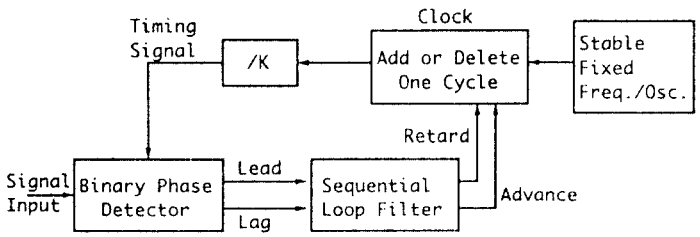

Fig. 5. The block diagram of the LL-DPLL scheme

Ⅳ. Design, Fabrication and Features of Clock Recovery Chip

1. Design of Circuits

This VLSI gate array chip is intended for use in the satellite ground system Modems. Its primary function is to adjust the frequency and the phase of a standard reference signal, to produce a clock signal. The recovered clock is used to process the received data. This chip will replace 30 LSTTL ICs. It uses 7 functional blocks to adjust the frequency and phase of a clock derived from a standard reference, to match the frequency and phase of the Pseudo Random data signal as Fig.6. The recovered clock allows optimum recovery of the data.

The data is applied to the I input of the mode selector, it detects positive and negative Data Transitions(DT), when the ACquisition Request(ACR) is active high. The positive edges of the loop selector and clock alarm to a fast acquisition mode. The system reset input resets the transition detectors to a low level output. It consists of two positive edge detectors and an edge detector.

The PD detects, whether the DT leads or lags the output clock. A LeaD pulse(LD) is generated when DT occurs in the positive half of output signal, and a LaG pulse(LG) is generated when DT occurs in the negative half of output signal. In high frequency applications, where external PD is used, the internal PD can be disabled by a high logic level on the EXternal PHase DETector(EXPHDET) input. The outputs of the external PD are connected to the appropriate EXLD, EXLG, EXDT inputs.

The basic function of the digital filter is to translate the lead and lag signals from the PD into phase control signals DLD, DLG that are more accurate and reliable than the inputs LD and LG. The digital filter accomplishes this translation statistically using a sequential Random Walk Filter(RWF). The sequential RWF operates on the principle that if equal numbers of pulses occur on LG and LD, then no output is produced, but if one has more pulses than the other, then DLD or DLG is produced. The digital filter consists of three serial counters, the first counter counts the LD pulses, the second counts the sum of (LG+LD) pulses, and the third counts the LG counter divided by M. For the correct operation of the digital filter, M must be greater than N but less than 2N. The actual divide ratios are set by the input Digital Filter Select(DFS). This sets the integration time of the filter, the larger the integration time, the more accurate are the DLD and DLG estimate and minimum jitter on output signal. A large integration time also means narrower

loop bandwidth. The outputs of the counters are detected using a negative edge detectors, which produce exactly one clock period pulse at DLD, DLG and the reset signal for the counters.

The loop selector controls the rate and the magnitude of the phase correction applied to the NCO. A pulse on the ACR input resets the loop selector and from this point, control signals are generated by counting the data transition. The DT are countered by a five-stage ripple counter and control signals are latched along the divider chain. There are basically four modes of operation. First control signal is gernerated which is active high for four data transitions. Its signal activates the ambiguity detector in the clock alarm circuit. Second control signal is gernerated which is active high for 24 DT and enables phase correction of the second programmable counter, which the lag and lead pulses directly from the PD. Third control signal is used to enable the phase correction of the first counter. Final control signal is active high for 32 DT, it disables the LG and LD pulses directly from the PD.

The NCO consists of two programmable counters: one divided by 3 counter and two divided by 2 counters. First programmable counter, nominally divided by 2 and the second programmable counter, nominally divided by 5. The NCO performs three basic operations. First, divides the high frequency reference by 120 or 60, when S60_120 input is low and high respectively. Second, the divide ratio can also be controlled by the lag and lead pulses from the loop selector. When LGC2 and LDC2 are present, the overall divide ratio changes from N to (N±4) respectively for one cycle of output clock. This can also be represented in term of 360/(N±4) degrees phase shift of output clock. Similarly, when LGC1 and LDC1 are present the overall divide ratio changes to (N ±1), phase shift of 360/(N±1) degrees. Finally, in order to support applications at higher speeds

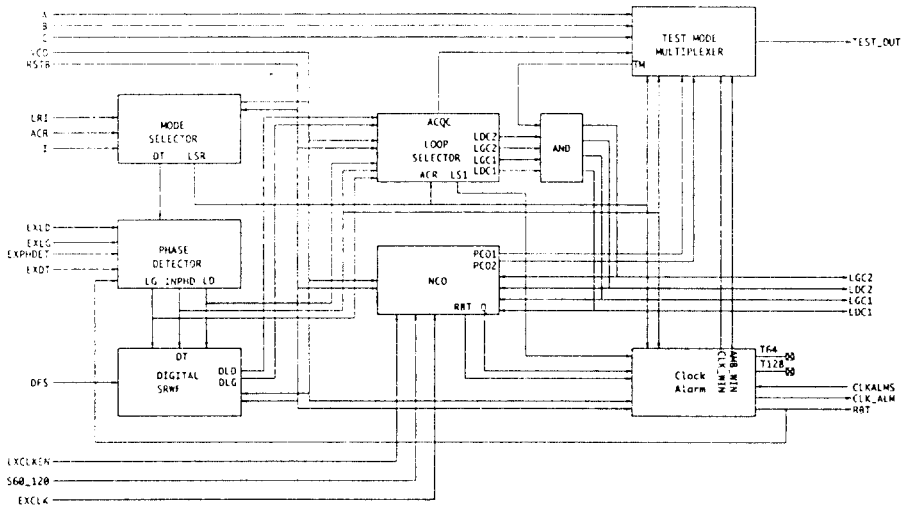

Fig. 6. The block diagram of the designed chip

than the gate array technology can support, external high speed programmable counters can be used, but since other functions are at lower speed, they can still be performed in the chip. In order to use external programmable counters, a EXternal CLocK(EXCLK) and EXternal CLocK ENable (EXCLKEN) inputs are provided. The output of the external counters can be fed in at EXCLK with EXCLKEN high and enabling the use of the reset of the chip. The external clock is six times the output clock.

The clock alarm circuit performs two main functions. Firstly, it monitors the position of the data transitions relative to the output clock and outputs a CLock ALarM(CK_ALM), if transitions are not within a certain CLocK WINdow(CLK_WIN). Secondly, it performs ambiguity detection, which is required to enable fast acquisition when data transitions are occurring within the AMBiguity WINdow(AMB_WIN). The clock window is a ±16.6% pulse of output clock, centered around the negative edge of output clock. The DT are phase compared to the clock window, which determines whether the DT are inside or outside the clock window. Since the DT are likely to have 50% timing jitter, the pulses inside and outside the clock window are integrated to give a more reliable indication of the relative position and hence produce a reliable CLK_ALM output. The ambiguity window is a ±16.6% of output clock, centered around the positive edge of output clock.

The function of the test mode multiplexer is to enable monitoring of the internal signals which are not available at the output pins. The test mode multiplexer consists of three control bits, allowing to multiplex eight signals, to one output pin(TEST_OUT). A special Test Mode(TM) is produced, which disables

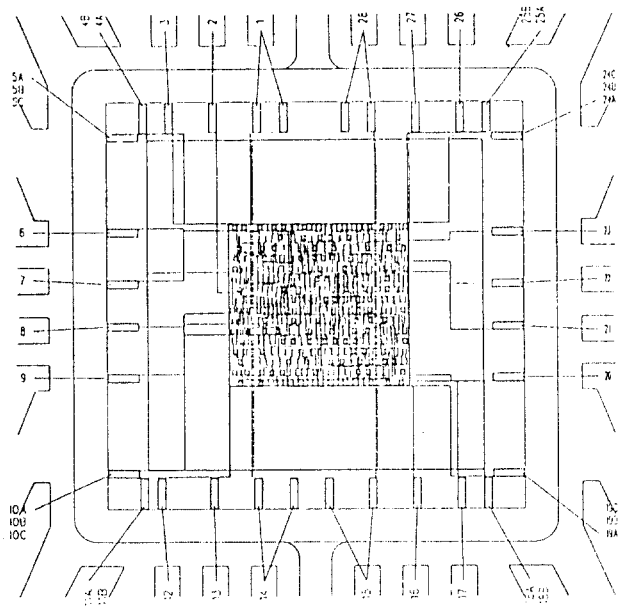

Fig. 7. The layout of place & routing

the corrections to the NCO, creating an open loop condition.

2. Physical Design and Fabrication

In the physical design process, we use the base array of the VGT300039 and SOG 1.0μm technology. This chip consists of 1,500 gates. The total power dissipation of the chip is maximum 100mW. The internal assigned power PAD is 2 pairs and the external one is 2 pairs. Fig.7 and Fig.8 show the results of place & routing and bonding diagram respectively. This chip is on was fabricated using 28pin plastic dual in line package shown as Fig.9 which is real-size picture.

3. Features of the chip

The chip consists of digital data transition

Table 1. Electrical characteristics

DC voltage (VDD)	Max +7V Min +2V
Power Dissipation	0.1W
Input Voltage	-0.5V~VDD+0.5V
Operating Temperature	0°C~70°C
Storage Temperature	-65°C~150°C
Input Current	10mA
High Level Output Ioh Current	4mA with 2V
Low Level input Iol Current	2mA with 0.2V
High Level input Vih Voltage	Min 2V Max 0.8V
High Level input Vil Voltage	Min 0V Max 0.8V
Input Leakage Current	150uA
Input Capacitance	50pF

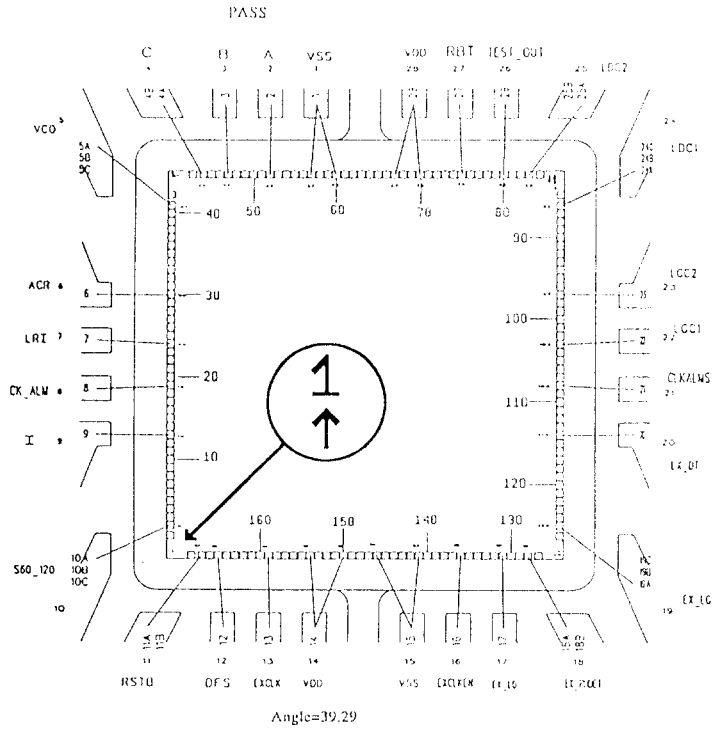

Fig. 8. The bonding diagram of the chip

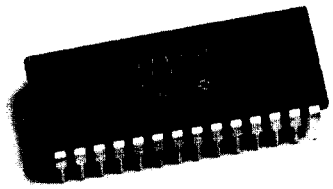

Fig. 9. The picture of fabricated chip in real size

tracking loop and operates up to data rate of 200Kpbs, with peak to peak phase jitter of ±3 degrees. The chip can be operate in burst or continuous mode in demodulators. It is compatible with LSTTL technology. The clock alarm indicates the status of the tracking loop. The loop bandwidth of the tracking loop can be selected. Electrical specifications of the chip show in table1. The table2 shows the information of input and output signals.

The maximum frequency on the VCO input is 20MHz with a rise and fall time of 5 *ns*. The maximum frequency on the TEST OUTput(TEST_OUT) pin when inputs A, B, C =1, 0, 0 is the VCO frequency divided by 2, and when inputs = 0, 1, 0 is the VCO frequency divided by 4. The timing information, which is relative to the maximum system clock frequency of 20MHz, is given in Fig.10. For other system clock rates, the clock periods should be adjusted appropriately. For VCO of 50 *ns* period with S60_120 input low (NCO divided by 120).

The loop filter was implemented using the sequential random walk filter which is very simple in its hardware. This filter consists of a 96 counter and two 64 counters. The filter bandwidth, which was represented in the equation (5), selected by the control signal in the counters. The part of VCO in APLL was designed by number controlled oscillator in digitally. Especially, hardware complexity is

Table 2. Device information and pin description

	Signal Name	Level	Active	Description
Inputs	LRI	TTL	High	loop reset input
	ACR	TTL	Low	acquisition request
	I	TTL		in-phase data
	EXLD	TTL	High	external lead pulse
	EXPHDET	TTL		external phase detector
	EXDT	TTL		external data transition
	EXLG	TTL		external lag pulse
	DFS	TTL		digital filter select
	CLKAMS	TTL		clock alarm test
	A	TTL		control bit for the test mode multipleexer
	B	TTL		〃
	C	TTL		〃
	S60_120	TTL		divide ration select
	EXCLKEN	TTL		external clock enable
	EXCLK	TTL	High	external clock
	VCO	TTL		master reference clock
	RSTB	TTL	Low	recovered bit timing
Outputs	LDC1	TTL		lead correction counter 1
	LDC1	TTL		lead correction counter 1
	LDC2	TTL		lead correction counter 2
	LDC2	TTL		lead correction counter 2
	RBT	TTL		recovered bit timing
	CLK_ALM	TTL		clock alarm out
	TEST_0	TTL		board level test out

Clock	signal	period	duty cycle	max rise	max fall
	VCO	50nS	high 20nS low 20nS	5nS	5nS

reduced by constructing simple programmable counters. Clock recovery loop is implemented by the concept of digital transition tracking loop and its divide ratio is selectable 60 and 120. In the table4, we show that the implemented chip can operate steadily up to 20MHz(VCO). For application over the speed of 20MHz, we use the hardware scheme which can operate connecting external PD and VCO. Clock alarm circuits and mode multiplexer produce useful information, which are monitoring the position of the data transitions relative to the output clock and the detection of ambiguity and monitoring of internal signals, for application systems. In the system applications, The designed chip not only can be

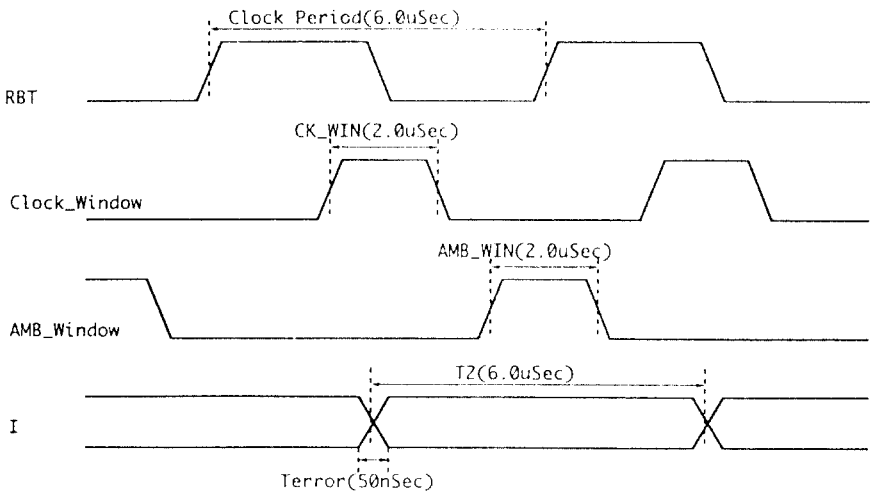

Fig. 10. Timing information of the chip

Table 3. Summary of design errors and warnings in pre-simulation

Massage Type	Errors	Warnings
Product	0	0
Utilization	0	0
Shorts	0	0
Dangling	0	0
Primary Signals	0	0
Level Shifter	0	0
Tree-State /Bus Repeater	0	0
Flip/Flop/Latch /Clock Buffer	0	0
Parallel Drive		
Total	0	0

Table 4. Pre & post-simulation results

Simulation Step	VCO Frequency	Error Rate(%)
Pre-Simulation	1MHz	0
	10MBz	0
	16MHz	0
	20MHz	0
	25MHz	3.98×10^{4}
Post-Simulation	1MHz	0
	10MHz	0
	16MHz	0
	20MHz	0
	25MHz	0.299

useful in continuous mode demodulators but also employed burst mode ones in such as TDM and ALOHA systems.

Ⅴ. Test Results and Performances

In back-end design, the fault coverage analysis shows 90.3%. The toggle coverage is 98.8% in the simulation using the test vector. The table3 shows the summary of design errors and warnings in pre-simulation. The results of pre & post-simulation is showed in the table4. This chip proved that its operating VCO frequency is up to 20MHz. In the real system, this chip was demonstrated its performance. System embeded test is perform in noise and no noise environment using 64Kbps VSAT continuous and burst demodulator in simulator and INTELLSAT VII links. In C/No = 56.6dB/Hz, the chip shows good performance and fast recoverying time within 1 byte.

Ⅵ. Conclusions

This paper shows analysis of clock recovery loop as a DPLL, then implementation schemes and features of one chip clock recovery. In addition to stable operation in noise environment, the chip designed using vgt300039 base and SOG 1.0μm technology not only demonstrates that its recovery time is within 1byte and phase jitter is $\pm$3 degree, but also shows good performance in embeded testing via satellite data links. It will be used at continuous and burst mode satellite or digital radio demodulation for clock and carrier recoverying up to 200kbps data and 20MHz system clock.

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