論文 96-21-7-13

A 3V-50MHz Analog CMOS Continuous time Current-Mode Filter with a Negative Resistance Load

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ABSTRACT

A 3V-50MHz analog CMOS continuous-time current-mode active filter with a negative resistance load(NRL) is proposed. In order to design a current-mode current integrator, a modified basic current mirror with a NRL to increase the output resistance is employed. The inherent circuit structure of the designed NRL current integrator, which minimizes the internal circuit nodes and enhances the gain bandwidth product, is capable of making the filter operate at the high frequency. The third order Butterworth low pass filter utilizing the designed NRL current integrator is synthesized and simulated with a 1.5μm CMOS n-well process. Simulation result shows the cutoff frequency of 50MHz and power consumption of 2.4mW/pole with a 3V power supply.

Ⅰ. Introduction

Several analog CMOS continuous-time active filters for high frequency applications have been reported in the literature[1]-[11]. Most of these active filters were designed to process voltage signals. It results in high voltage power supply and large power dissipation. In order to overcome these drawbacks of the voltage-mode filters[1, 2, 4, 6] the current-mode filter circuits, which process current signals, have been developed[3, 5, 11]. Current-mode signal processing is potentially faster than voltage-mode signal processing because parasitic capacitance effects in high impedance circuits is more severe than parasitic inductance effects in low impedance circuits[3]. Since a magnitude of current with a low voltage of power supply can be controlled in current-mode circuit, a low power dissipation can be achieved. Some of these current-mode filters have employed cascode current mirrors to implement a current integrator. However, four stacked transistors in the current integrator require a high voltage of power supply. And many internal nodes prevent the current integrator from operating at very high frequency range.

In order to reduce a magnitude of power supply voltage, an NRL current integrator is proposed to design a current-mode low pass filter for high frequency application. The NRL current integrator, which is the counter part of the voltage-mode NRL integrator[4, 11], consists of basic current mirrors and negative resistance loads to generate not only high impedance nodes, but also a minimum number of internal nodes.

Ⅱ. The Modified Current Integrator with an NRL

A circuit diagram of the differential input/differential output NRL current integrator with basic current

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論文番號:96026-0125
接受日字:1996年 1月 25日

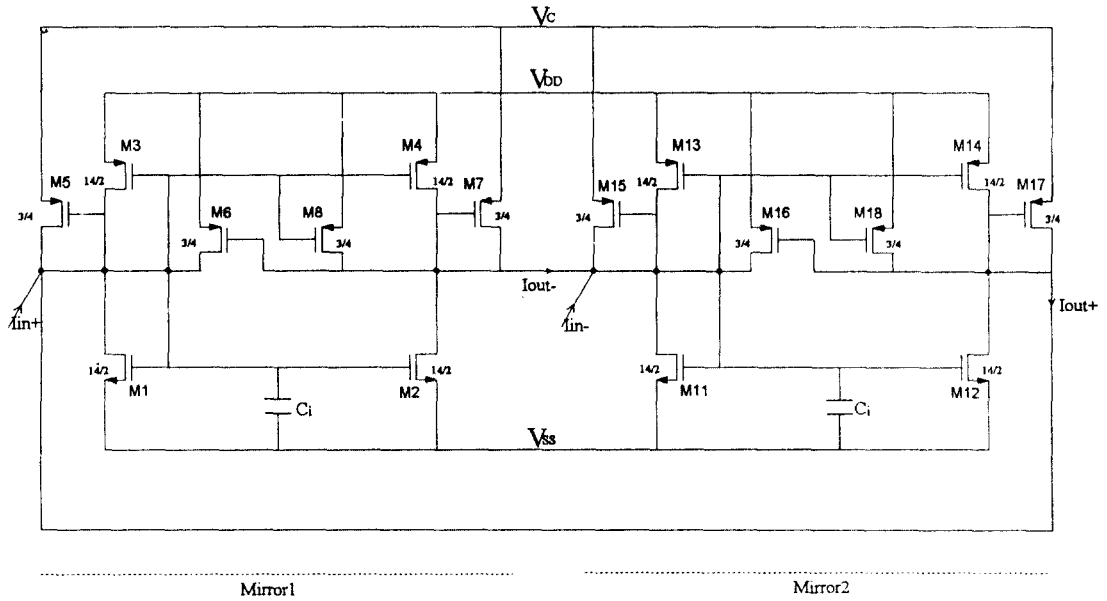

Fig 1. The circuit schematic of the designed NRL current integrator

mirrors is shown in Fig. 1. The integrator consists of two modified basic current mirror circuits, mirror1 (M1, M2, M3, M4) and mirror2(M11, M12, M13, M14), and two NRL circuits(M5, M6, M7, M8 and M15, M16, M17, M18).

The current gain transfer function of the integrator in (1) can be obtained by analyzing the small signal model for the half circuit of the NRL current integrator, as illustrated in Fig. 2

$$\frac{I_{out}}{I_{in}} = \frac{g_{m,\,out} - g_{ds,\,out}}{g_{ds,\,in} + g_{ds,\,out}} \cdot \frac{\left(1 - s\,\frac{c_O + 2c_B}{g_{m,\,out} - g_{ds,\,out}}\right)}{\left(1 + s\,\frac{c_i + c_O + 4c_B}{g_{ds,\,in} + g_{ds,\,out}}\right)}$$

$$= A\,\frac{\left(1 - \frac{s}{z_1}\right)}{\left(1 + \frac{s}{p_1}\right)} \qquad (1)$$

, where

$$c_O = c_{gs6} + c_{gs7} + c_{bd2} + c_{bd4} + c_{bd7} + c_{bd8} \approx c_{bd2} + c_{bd4},$$
$$c_B = c_{gd2} + c_{gd4} + c_{gd6} + c_{gd8} \approx c_{gd2} + c_{gd4},$$

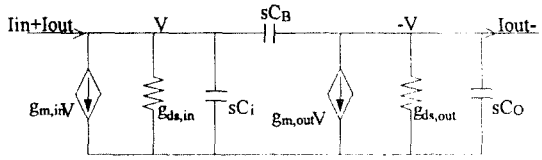

Fig 2. The small signal equivalent circuit of the half circuit of the current integrator

$$g_{m,\,in}(=g_{m1}+g_{m3}) \approx g_{m,\,out}(=g_{m2}+g_{m4}),$$
$$g_{ds,\,in}(g_{m5}-g_{m6}+g_{ds1}+g_{ds3}+g_{ds5}+g_{ds6})$$
$$\approx g_{ds,\,out}(g_{m7}-g_{m8}+g_{ds2}+g_{ds4}+g_{ds7}+g_{ds8})$$

, A is the dc current gain, P_1 is the dominant pole, and Z_1 is the zero.

Two gate to drain connected transistors(M1, M3 or M11, M13) in each mirror, are employed to increase a transconductance of each mirror that is each current amplifier, and consequently, a bandwidth of the integrator. As the zero point, Z_1 is proportional to the transconductance $g_{m,\,out}$ of each mirror, the bandwidth can be enhanced by $(1+g_{m4}/g_{m2})BW_O$,

where BW_O is the bandwidth of the integrator utilzing the basic current mirror that has only one gate to drain connected transistor. The designed circuit takes advantage of the bandwidth enhancement at the expense of the relatively large dc voltage drop, $2V_{dsat}+2V_{th}$ across M1 and M3 rather than that of the basic current mirror, $2V_{dsat}+2V_{th}$. Another advantage of utilizing two gate to drain connected transistors is that it does not require the extra bias circuit.

Ⅲ. Negative Resistance Load

Another problem of employing the basic current mirror in the current integrator is that the dc current gain of the integrator is unable to exceed 40 dB due to the dc current gain of $(g_m/2g_{ds})$[5]. The proposed current NRL circuit is capable of enhancing the dc current gain of the integrator over 60 dB. The MOS transistors (M5, M6, M7 and M8) construct a current NRL circuit. Because the current integrator operates in the differential mode, the input node voltage possesses the same magnitude of the output node voltage with the opposite sign. Applying KCL to the input and output nodes of the mirrorl circuit, (2) and (3) are obtained as:

$$I_{in}+I_{out}=(g_{m1}+g_{m3}+g_{m5}-g_{m6}+g_{ds1}+g_{ds3}+g_{ds5}+g_{ds6})V$$
$$=(g_{m1}+g_{m3}+g_{ds,in})V \quad (2)$$

$$I_{out}=(g_{m2}+g_{m4}+g_{m7}-g_{m8}+g_{ds2}+g_{ds4}+g_{ds7}+g_{ds8})V$$
$$=(g_{m2}+g_{m4}+g_{ds,out})V \quad (3)$$

In (2) and (3), two terms, $(g_{m5}-g_{m6})$ and $(g_{m7}-g_{m8})$ can be rewritten by;

$$g_{m5}-g_{m6}=g_{m7}-g_{m8}=\mu_p c_{ox} S_5(V_C-V_{DD}) \quad (4)$$

, where S_5 is the device aspect ratio of the MOS transistor, M5.

The NRL can be achieved by making V_C smaller than V_{DD}. The proper tuning of V_C makes it possible to satisfy (5).

$$\mu_p c_{ox} S_5(V_{DD}-V_C) \approx g_{ds1}+g_{ds3}+g_{ds5}+g_{ds6} \approx g_{ds2}$$
$$+g_{ds4}+g_{ds7}+g_{ds8} \quad (5)$$

In other words, $g_{ds,in}$ and $g_{ds,out}$ can be made to be close zero. The resultant dc current gain of the NRL integrator is $(g_{m2}+g_{m4})/(g_{ds,in}+g_{ds,out})$ and can be ideally reached to the infinity. In order to generate the large dc current gain, it is required to generate the smallest value of $(g_{ds,in}+g_{ds,out})$ as possible. To make it occur, two parameters, S_5 and V_C in (5) need to be finely controlled.

Ⅳ. Active Filter Synthesis

A 3rd order Butterworth low pass filter with the bandwidth of 50MHz has been realized by employing the designed NRL current integrator. The doubly terminated third order passive low pass filter, as shown in Fig. 3, is utilized[12] to synthesize the associated active filter, as illustrated in Fig. 4. The integrators(INT1, INT2, INT3) are the identical NRL current integrator designed in Fig. 1. In the synthesized active filter circuit, it is noted that the output of the integrators is connected to the input of the adjacent integrator. The connection is achieved by adding an extra current mirror to the designed NRL integrator circuit.

The dominant pole, P_1 and the gain-bandwidth product, P_1A of the NRL current integrator are controlled by the input integration capacitor, C_1, as shown in (6),

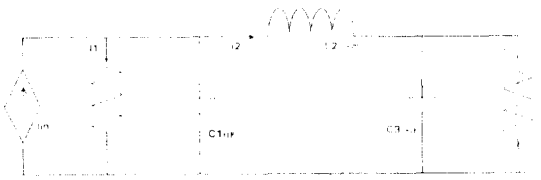

Fig 3. A circuit diagram of the third order passive Butterworth low pass filter

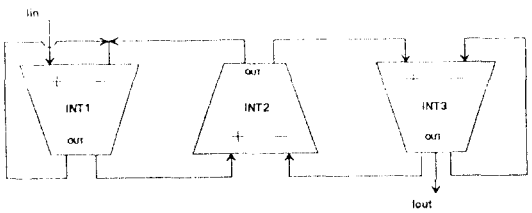

Fig 4. A block diagram of the current-mode ontinuous-time NRL active filter

$$C_i = \frac{g_{mi,\,out} X_{normalized}}{2\pi f_O} - C_{parasitic} \quad (6)$$

where $C_{parasitic}$ is a parasitic capacitance equal to $C_O + 4C_B$ on the input node of the integrator, $g_{mi,\,out}$ is a transconductance of the modified basic current mirror, f_O is the mapping frequency, and $X_{normalized}$ is each normalized element value of passive network.

V. Simulation results and Discussions

The frequency responses of the NRL current integrator are plotted in Fig. 5 as a function of V_C(2.76V, 2.77V, 2.78V, 2.79V). The condition of V_C equivalent to 2.76V is shown to satisfy (5) to generate the highest dc current gain of the designed NRL current integrator. The frequency response of the conventional cascode current integrator is also compared with those of the NRL current integrator in Fig. 5. The simulation results show that the frequency response of the conventional cascode current integrator is similar to that of NRL current integrator with V_C of 2.78V. The harmonic distortions of the cascode and NRL current integrators are plotted in Fig. 6 and Fig. 7. It is noted from the simulation data that the harmonic distortions of two circuits are similar. The magnitude Bode plot of the third order active filter as a function of V_C is shown in Fig. 8. The zoomed plot in the box illustrates the variation of V_C which rarely affects the frequency response of the designed active filter. The simulation results of the active filter are summarized in Table 1. It shows the cutoff frequency of 50MHz and power consumption of 2.4mW/pole with a single power supply of 3V. The electrical performances of the designed active filter are compared with those of

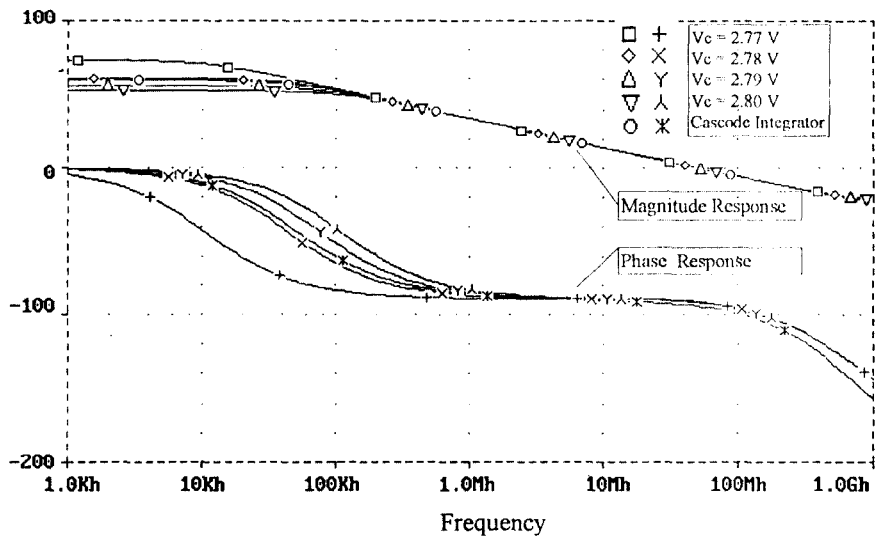

Fig. 5. The frequency response of the designed NRL current integrator(V_C : the external tuning voltage)

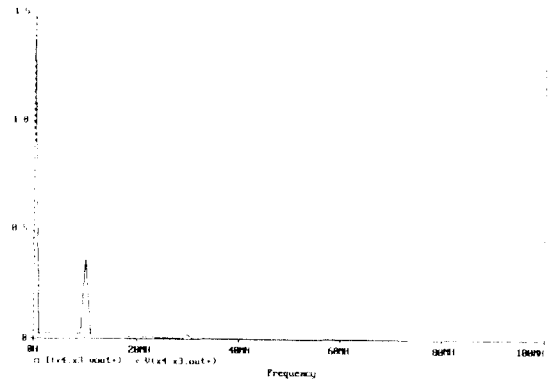

Fig. 6. The simulated harmonic distortion response of the conventional cascode current integrator

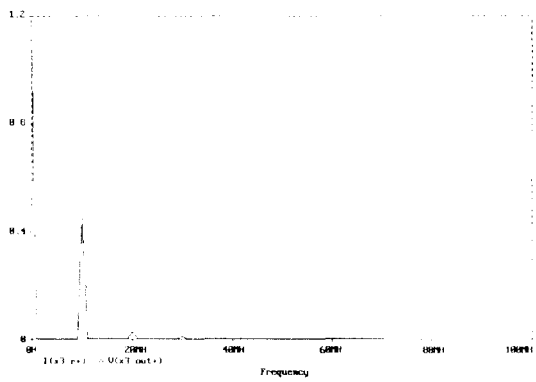

Fig. 7. The simulated harmonic distortion response of the NRL current integrator

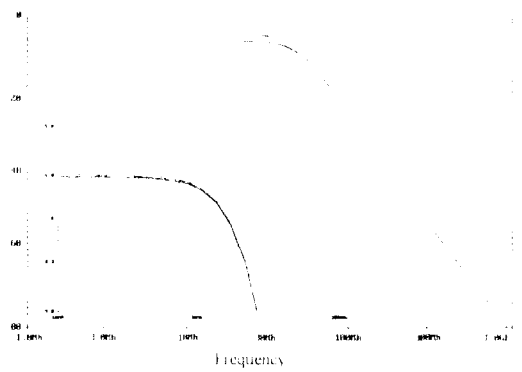

Fig. 8. The frequency response of the designed third order Butterworth low pass current-mode NRL active filter with the bandwidth of 50MHz

Table 1. Simulation results of the current-mode NRL active filter

Process	CMOS n-well 1.5μm
Power Supply	3V
3dB cutoff frequency	500MHz
Power Dissipation	2.4mW/pole
Active Transistor Gate Size	560μm^2/pole

the other voltage-mode and current-mode active filters, as shown in Table 2. The proposed NRL current-mode filter requires a relatively lower power consumption for a comparable bandwidth than other

Table 2. Comparison of the electrical performances of the active filters

	A Linear..[11]	A CMOS..[5]	A 3V-125..[4]	This paper
Power Supply	5V	5V	3V	3V
Power Consumption	2.7mV/pole	11mW/pole	6mW/pole	2.4mW/pole
Bandwidth	50MHz	63MHz	125MHz	50MHz
The position of parasitic pole or zero	100GHz	10GHz	900GHz	1GHz
Process	2μm CMOS	3μm CMOS	1.2μm n-well CMOS	1.5μm n-well CMOS
Building Block	gm-C	gm-C	Current Integrator	Current Integrator

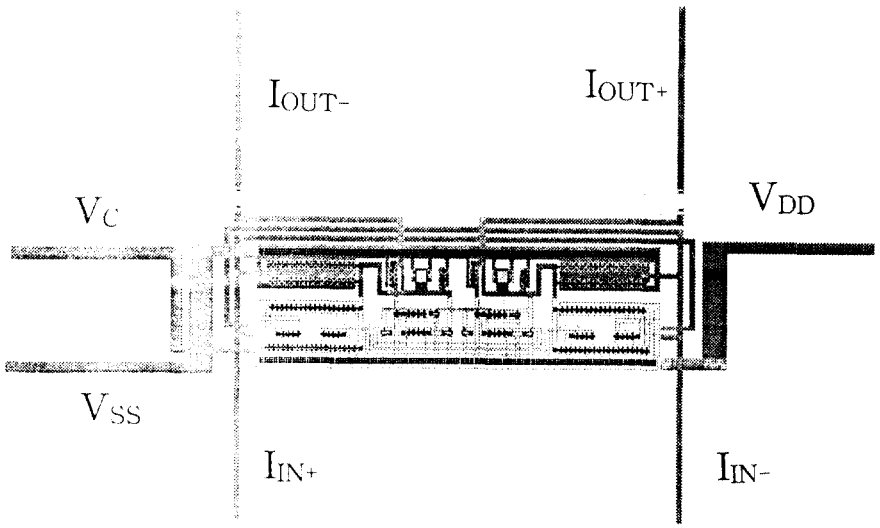

Fig. 9. The layout of the current-mode NRL integrator

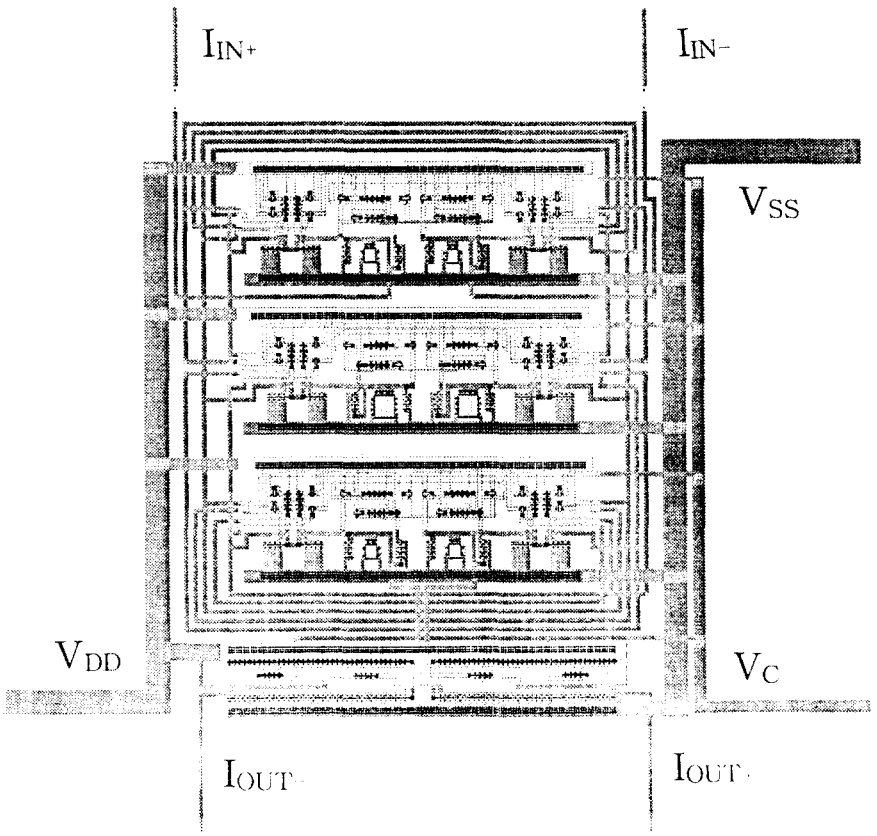

Fig. 10. The layout of the current-mode NRL active filter

active filters. The layout of the current-mode NRL integrator and filter are illustrated in Fig. 9 and Fig. 10, respectively. The chip size of the NRL current-mode filter is 0.9mm x 0.9mm.

Ⅵ. Conclusions

A current-mode NRL integrator is designed to implement the third order Butterworth low pass filter with the bandwidth of 50MHz. Since the designed integrator consists of the modified basic current mirrors and NRL circuits, it requires a low voltage (3V) and a low power dissipation(2.4mW/pole). The inherent circuit structure, which minimizes the internal circuit nodes and enhances the gain bandwidth product, makes the current-mode NRL filter be capable of operating at the high frequency. The simulation results show that the frequency response of the proposed current-mode NRL integrator is similar to that of the conventional cascode current integrator and the current-mode NRL filter requires a relatively lower power consumption for a comparable bandwidth than that of the other active filters.

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