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SPICE Models of PCB Traces in High-Speed Systems

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고속 시스템에서의 PCB 선로의 SPICE 모델

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ABSTRACT

Physical interconnect such as Printed Circuit Board(PCB) traces introduces new challenges for parameter extraction and delay calculation for high-speed system design. PCB traces are dominated by frequency dependent LC propagation which makes precharacterization difficult for all possible configurations. Moreover, simulating the transient behavior of the trace for noise and delay analysis requires the combined use of a variety of models and techniques for efficiently handling lossy, low-loss, frequency dependent, and coupled transmission lines together with lumped elements. In this paper we explain how the frequency dependence caused by ground plane proximity and skin effects can be modeled using the abstracted models. these abstracted (lumped) models are SPICE-compatible and can be simulated in time-domain, along with precharacterized lumped parasitic elements and nonlinear driver and load models.

요 약

인쇄회로기판상의 트레이스와 같은 물리적 신호선들은 고속 시스템 설계를 위한 변수 추출 및 시간 지연 계산 시에 문제가 되어 가고 있다. 인쇄회로기판 트레이스는 주파수 의존적인 LC전파에 해당하기 때문에 설계 전단계에서의 특성화가 어렵다. 게다가 잡음 및 지연 해석을 위하여 트레이스 과도응답을 해석하는 일은 집중소자들과 함께 저손실, 주파수 의존적인 결합 전송선을 효율적으로 시뮬레이션해야 하기 때문에 여러 모형과 해석 기법들을 혼용하여야 하는 문제가 발생한다. 본 논문에서는 접지평면의 근접 및 표피효과에 의해 야기되는 주파수 의존성을 추상 모형을 이용하여 어떻게 모형화하는 가를 보였다. 이렇게 추상화된 (집중)모형은 SPICE와 양립성이 있으며 미리 특성화된 집중 기생 소자, 비선형 구동 회로 및 부하와 함께 시간영역에서 시뮬레이션할 수 있다.

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Ⅰ. Introduction

For system-level designs, such as multi-chip modules (MCMs) and printed circuit boards(PCBs), the interconnect is becoming a dominant factor for signal integrity since there can be considerable delays due to transmission line effects. In addition, noise can have a dramatic impact on the settling time of a net, thereby determining the maximum rate at which the interconnect can be reliably clocked. In general, the interconnect delay and the coupled signal noise must be considered together as they impact the overall "system delay".

To model interconnect effects, the electrical circuit parameters must first be extracted then simulated with the proper nonlinear driver and load models. In general, low-to mid-performance system designs, such as medium-and large-size PCBs, can avoid some of these costly simulations by using well-chosen design rules and simple engineering models. High-performance, high-speed systems, however, such as MCMs and small PCBs, must be designed using manual trial-and-error with an extractor and simulator.

In semiconductor design area, the methodology of efficient, yet accurate extraction and fast simulation has been regarded as one of vital elements for high-performance chip designs. Since the barrier dividing chip design and system design has been disappearing due to the technology evolution, it is evident that this conjecture will soon be prevalent even in system design. Moreover, there has been an interest in developing the method of producing a high-performance MCM or PCB in a reasonable amount of time. One key part of this process is the efficient extraction and simulation of MCM and PCB interconnect in an automated fashion. This paper details an approach to providing such capabilities.

Following this introduction, in Section 2 we explain an approach for generating very accurate circuit models for trace cross-sections commonly found in MCMs and PCBs. This approach uses conformal mapping to directly generate abstracted RLC library models which capture frequency dependence, proximity effect, and coupling in terms of equivalent circuit models. In Section 3, it is shown that an extension of the Method of Characteristics (MC) techniques, which can be directly plugged into any SPICE netlist, captures frequency-dependent effect of PCB traces. An automatic technique of generating this SPICE models is proposed which selects the most efficient simulation model for a given portion of a net. In this framework, non-linear effects, such as diode terminations and nonlinear drivers which can be shown to significantly impact the noise and settling time, can be included in the time-domain analysis. In Section 4, the concluding remark is given.

Ⅱ. Parameter Extraction

A critical issue in the development of efficient models for the extraction and simulation of interconnects is their consistency with Maxwell's equations. For a long interconnect, (i.e., one for which delay is long compared to rise time), extracted parameters must not only predict rise times at the load end, but also predict causal delays. Considering the dimensions of practical interconnect structures and the rise time of even very high speed digital signals, the mode of propagation is quasi-TEM. Thus, quasi-static analysis of the structure should provide sufficiently accurate results[16].

For the quasi-static model, both the resistance and the inductance values depend on frequency, and are not independent of each other. At low frequency, the current is uniform throughout the cross-section of the conductor, which has an effect on the low frequency inductance. However, at high frequency, the current distribution is determined by the external inductance (i.e., currents redistribute in such a way that total inductance is minimized). This current crowding to the surfaces of the interconnect in closest proximity to the ground return increases the resistance. Skin-effect,

which is driven by the internal inductance of the conductors, can also be viewed in a similar manner. Since a high speed digital pulse has a wide bandwidth from dc to the order of $1/t_r$, where t_r is the signal rise time, the parameter extraction model used should include all of these effects, efficiently and accurately.

Generating abstracted, or analytical electrical-parameter models for geometries used in interconnect structures is not trivial even for quasi-static calculations. Using an appropriate conformal map, the complexity of the problem can be reduced. Conformal mapping solutions are exact for perfect conductors, once the map is obtained. The application of conformal mapping to the calculation of the complex internal impedance of conductors is less well known[10]. In general, consider a conformal map $f(z)$ (where $z=x+jy$ is the real space domain), which produces parallel plates in the mapped domain, $w=u+jv$, with plates parallel to u-axis and separated by v_0. For a single conductor along with a ground-plane, the conformal map gives a transformation of the form shown in Fig. 1.

The scale factor M relating a differential length in the z-plane to one in the w-plane is given by

$$M(u, v)=\left|\frac{df}{dz}\right|_{u, v} \tag{1}$$

With the surface impedance (Z_S) of stand-alone conductor, the total series impedance per unit length for the transmission line, including the impact of finite resistance and current crowding is given by

$$Z(\omega)=\left[\int_0^{u_0}\frac{du}{j\omega\mu_0 v_0+Z_S M(u, v)}\right]^{-1} \tag{2}$$

Skin-effect resistance can be included through the surface resistance expression. For a parallel plate transmission line, the surface impedance of the conductors is given by $Z_0/\tanh(\gamma t)$, where Z_0, γ and t are the characteristic impedance, complex propagation constant in the conductor, and the thickness of the conductor, respectively. The surface impedance of rectangular conductors are more tedious to calculate. For this case fields are not only at one side, but all around the conductor. To calculate the surface impedance, we partition the conductor into 4 pieces, two triangles and two trapezoids with 45 degree angles at their bases as shown in Fig. 1. Then each segment can be treated as a non-uniform transmission line in the lateral direction [15], and the surface impedance can be calculated readily.

As an example, consider the microstrip example in Fig. 2. The conductor is partitioned as described above and the contributions from the different partitions are distinguished and represented by a three stage ladder. One ladder for the lower trapezoid, one for the upper, and one for the remaining two triangles, Each ladder consists of a series inductance and a two ladder skin-effect model. The equivalent circuit model that captures both proximity effect and skin effect, and lumps the interconnect in the transverse direction for the cross-section in Fig. 2 is shown in Fig. 3.

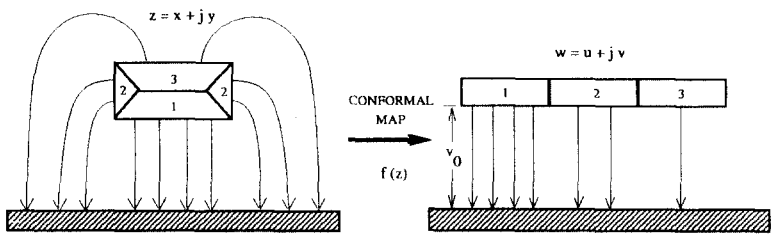

Fig. 1 Transformation of a single line conductor along a ground plane using the conformal map $f(z)$.

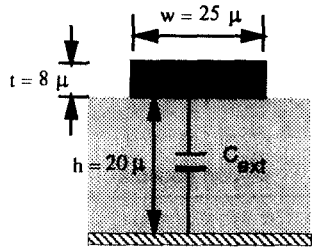

Fig. 2 Example of a typical MCM microstrip line.

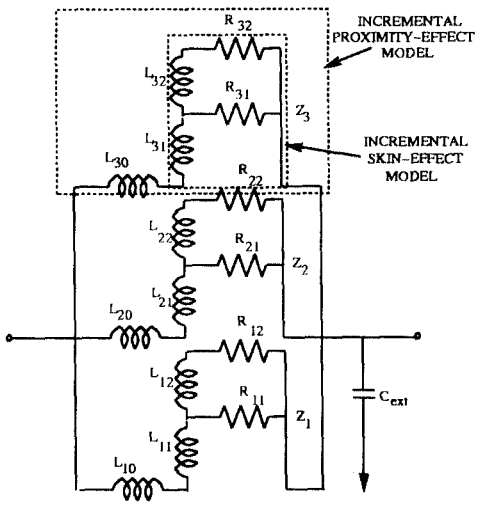

Fig. 3 An elementary cell modeled from the proposed extraction method.

Directly simulating this ladder for every incremental transmission line segment would be an enormous task for a time-domain simulator. However, this model can be reduced to either a 4-element circuit or a 2-element circuit (2 R's and 2 L's) as illustrated in Fig. 4 without compromising accuracy. Using RICE[12], an interconnect-specific version of AWE, a stable 2nd-order $\tilde{Z}(s)$ for this RL-ladder can be generated. Then, the second order circuit in Fig. 4(a) can be synthesized using the first Cauer-form, which is obtained through the continued fraction expansion of the impedance about $s=\infty$. It can be shown that this synthesis is guaranteed to produce a passive circuit for 2nd order [11]. Examples in Section 4 shows that the variation of inductance and resistance with frequency is readily captured with a 2nd order model. The first Causer form is used since it results in the high frequency inductance, L_1, isolated from the other elements as shown in Fig. 4(a). We will see that this is extremely important for handling frequency dependence with the method of characteristics.

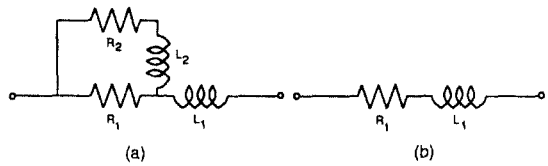

Fig. 4 A second (a) and a first (b) order model of the 15-element cell in Fig. 3.

Ⅲ. Efficient SPICE Models

Once we have the RLCG transmission line parameters of PCB traces, there are various techniques which can be applied to solve for the time-domain waveforms. Most analyses involve either a distributed model [13, 14] or a lumped equivalent circuit model [5, 8]. Both types of analysis have there strong and weak points.

Lumped equivalent models such as Iterative Ladder Circuit (ILC) models are efficient for lossy interconnect lines, and beneficial in that they are directly compatible with nonlinear driver and load models. Lumped models become inefficient when the lines are long or low-loss since the increased number of lumps results in a bigger matrix problem. Increasing the number of lumps also results in larger pole values which may force the integration time-step to become smaller to avoid unwanted numerical oscillations.

Distributed models which are derived from the solutions of partial differential equations capture the effects of low-loss lines efficiently [13], however, they are generally more difficult to interface with nonlinear drivers/loads and interconnect discontinuities. Exten-

sions have been made to incorporate loss effects by combining (AWE) [1, 17] and the Method of Characteristics (MC) [2]. Simple extensions have also been tried by segmenting the MC model into several sections in order to distribute the series resistance [9]. For low-loss lines, this model can be extremely simple and efficient.

The extension of the above approach is explained in this paper. First, frequency dependent effects are captured in the elementary cell model as shown in Fig. 3, and then transformed to the first Cauer-form of 2nd order. This synthesized model is then embedded in an extended form of MC models to be plugged in SPICE netlists. The necessary number of MC cells are used to properly distribute the small amount of series resistance.

1. Single, Uniform Low-loss or Lossless Traces

In spite of the simplicity of ILC models, the pure lossless system is unquestionably best described by the method of characteristics. The method of characteristics can be extended to lossy lines using the segmenting method in [6]. However, the main disadvantage with this approach is that it involves convolution, which generally increases the complexity of time-domain analysis. In addition, the required number of MC sections increases as the line becomes lossier.

Segmenting the MC model involves cascading several lossless lines with losses inserted as lumped elements between them as shown in Fig. 5.

Note that the high frequency inductance term, L_1 (Fig. 5), is used to characterize the ideal delay of the cell. This permits the modeling of frequency dependence with the method of characteristics. The stencils for the circuit model based on the method of characteristics can be derived directly from the equations described in [2], and are shown in Fig. 6.

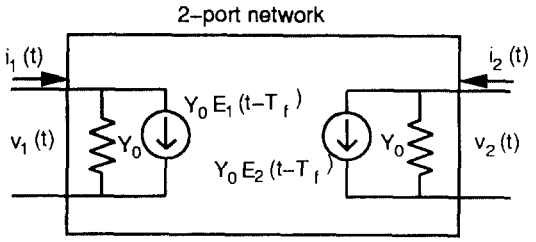

Fig. 6 Time-domain stencil for the MC-models of lossless lines.

State variables in Fig. 6, E_1 and E_2, are given by Eq. (3), and can be implemented using circular queues [1].

$$E_1(t) = -[2v_2(t) + E_2(t-T_f)]$$
$$E_2(t) = -[2v_1(t) + E_1(t-T_f)] \quad (3)$$

The frequency dependencies discussed in Section 2 can also be incorporated into MC-models. With the reduced-order cells shown in Fig. 4, either 1st-or 2nd-order MC-macromodels can be generated by building the loss-less cell with the synthesized, per-unit-length L_1 and C_1. For the 2nd-order model, the inserted loss in MC-models is composed of 2 R's and 1 L's (R_1, R_2 and L_2 in Fig. 4(a)).

As the loss is increased, more MC-cells are needed to accurately capture the time-domain response. The time-step size must be made smaller as the number of MC-cells is increased since the resolution of the time-of-flight queues is smaller. Therefore, it is useful

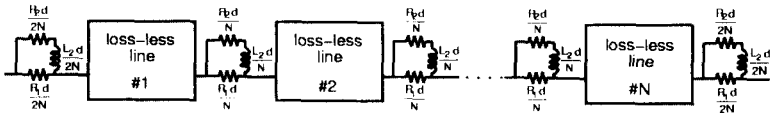

Fig. 5 Modeling low-loss lines with the combination of pure lossless-line cells and lumped losses.

to compare the error of the ILC-models as the loss is decreased with the error in the MC-model as the loss is increased. Starting with the *ABCD* matrix of a MC-cell with $R_t/2N$ at cell terminal, we can generate the equivalent *y*-parameter matrix [11]. From these *y* -parameters we generate an error plot as shown in Fig. 7. Note from Fig. 7 that the bandwidth for MC-models under a given error tolerance decreases as the line becomes lossy.

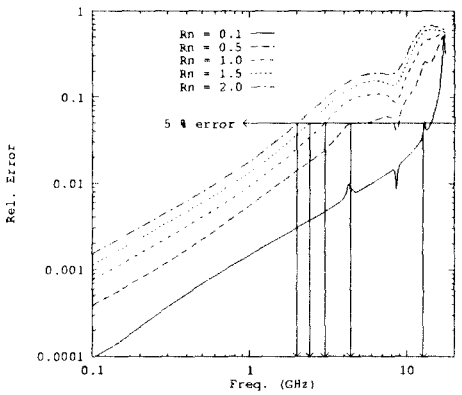

Fig. 7 Relative errors on $y_{11}(s)$ of the MC model, $\varepsilon_{y_{11}}{}^{MC}(\omega_n, R_n, N)$, for a line ($T_f = 60$ *ps*) when $N = 2$.

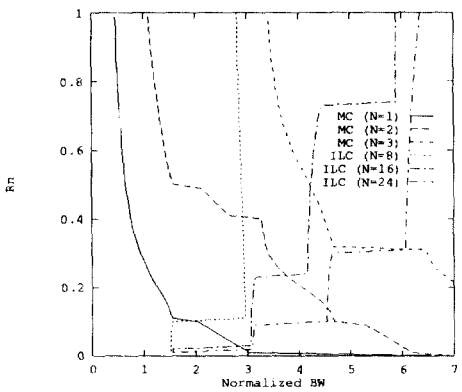

Fig. 8 Line loss versus bandwidth curves for both ILC-and MC-models when the error tolerance is 5%.

Roughly speaking, for an MC queue size of 10, the runtime complexity of a single MC cell is approximately equal to the complexity of an 8-cell ILC. Therefore, we can plot the loci of both ILC and MC cells for R_n(normalized resistance) versus $\omega_n{}^{max}$(normalized maximum angular frequency) with respect to an error of 5%, as shown in Fig. 8. Note that these loci are generated by sweeping the error equation over $\omega_n{}^{max}$ for a fixed value of R_n. Since an 8-cell ILC is roughly of the same complexity as one MC-cell, a boundary can be established from the intersection of various loci plots. Therefore, given the line parameters, an optimal model can be efficiently selected.

2. Multiple, Uniform Coupled Traces

The simulation models presented here can incorporate both inductance and capacitance coupling. Under the quasi-static assumption, it is well known that coupled-lines in a homogeneous medium can be decoupled using the congruence transformer [3], which can be implemented by a set of linear controlled sources [5, 7]. A schematic diagram of the decoupling is shown in Fig. 9. Once decoupled, the lines are simulated using the models explained in the previous section.

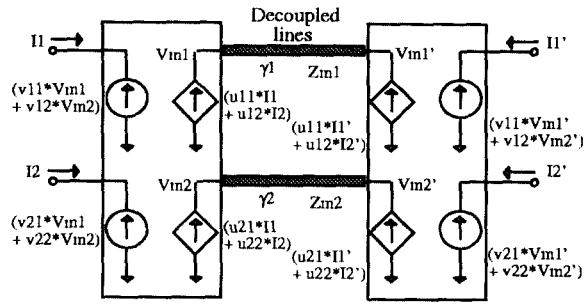

Fig. 9 Schematic diagram of decoupling method for coupled lines under quasi-static assumption. $[v_{ij}]$ is the voltage eigen-vector matrix and $[u_{ij}]$ is the inverse of the current eigen-vector matrix.

We should add, however, that coupled lines with frequency-dependencies cannot, in general, be decoupled with a real transformation matrix [5]. If the transformation matrix is complex, the evaluation of node

variables during simulation will require a complicated convolution procedure. In this case, we calculate the *ABCD* parameters for the coupled lines symbolically using the chain rule [4], and convert this *ABCD* parameter matrix into the *y*-parameter matrix, which is used to generate time-domain stencils. It is worthwhile to note that this approach guarantees unconditional stability since no artificial model-order reduction technique, such as *Padé* approximation, has been involved in the model derivation process, and the network descriptions are obtained from finite, physical, passive networks. This property is contrasted with the approach in [4], where the instability problem of *Padé*-synthesized characteristic impedance network has been reported.

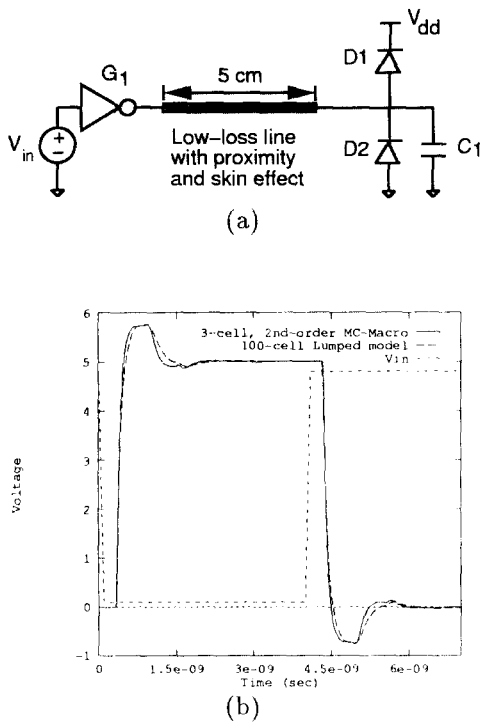

Fig. 10 Example circuit configuration of the frequency-dependent line with nonlinear driver and load ($C_L = 1\ pF; t_r = 100\ ps$).

3. Simulation Results

A 5 *cm* long, low-loss trace, the structure of which is shown in Fig. 2, has been modeled using 3-cell MC-model for 5% error tolerance. In Fig. 10, a nonlinear driver and diode terminations are added to this trace. The capacitance at the far-end represents the total sum of solder bump and input load capacitances. This circuit configuration was simulated using 3-cell, 2nd-order MC-model and compared against the 100-cell lumped model since more than 100 lumped cells were required to yield less than 5% error tolerence. The CPU time for the lumped model was 1336 times larger than that for the MC-model.

Ⅳ. Conclusions

This paper presents a unified framework for extraction and simulation of PCB traces with the objective of estimating a system-level timing information that is accurate and efficient enough for design activities. We propose an efficient, yet flexible, approach for parameter extraction based on conformal mapping and representation of frequency dependencies, such as skin-effect and proximity effect, in the form of equivalent circuit-models. Depending on the relative line loss, the normalized maximum angular frequency and the error tolerance of analysis, either traditional iterative ladder circuit models or proposed MC models can be used for the most efficient SPICE models of the given PCB traces. These SPICE models not only address the instability problem during simulation, but also provide the simplicity for varying the simulation accuracy and efficiency.

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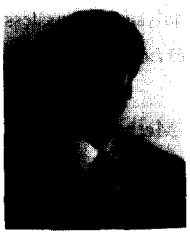

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