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# Mean Time Delay Variation Performance of DTTL Bit Synchronizer

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# DTTL 비트동기장치의 평균시간지연 편차 성능에 관한 연구

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ABSTRACT

The measured pulse shapes provided in the given data package demonstrated pulse distortions due to laser speckle. The distorted pulse shapes were carefully analyzed, modeled, and then applied to the DTTL(Digital-data Transition Tracking Loop)[1] bit synchronizer simulator to measure the mean time delay and its delay variation performance. The result showed that the maximum mean time delay variation with the modeled data was 12.5% when window size equals 1. All the data given were located within this modeled boundary and the maximum mean time delay variation was 7% in this case. The mean time delay variation was known to be smaller by reducing the window size[2][5][6]. The mitigated delay variation was 2.5% in the modeled case and 1.4% in the data set given when the window size equals 0.1. With the digital DTTL instead of analog DTTL, similar result was obtained.

요 약

실험결과 주어진 데이타묶음에서는 레이저 speckle에 의한 파형왜곡들이 있었다. 이 파형을 면밀히 분석하고 모델링한 후, DTTL[1] 비트동기장치에 인가하여 평균시간지연과 평균시간지연편차 성능을 측정하였다. Window 크기가 1일때의 실험 결과, 모델링된 pulse의 경우 최대 평균시간 지연편차가 12.5%였다. 제공된 data는 모두 모델링된 pulse의 왜곡범위 내에 있었으며, 이 경우 최대 평균시간지연편차는 7%를 보였다. 평균시간지연편차는 window 크기를 축소함으로써 작아진다고 알려져 있다[2][5][6]. Window 크기가 0.1 일 때 편차는 모델링된 경우 2.5%, 제공된 data의 경우 1.4%로 줄었으며, DTTL 비트동기장치의 디지탈 구현에 의한 측정결과도 아날로그 구현의 경우와 유사하였다.

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## Ⅰ. Introduction

Bit synchronization is used to describe the problem of estimating the time instant at which the modulation can change its state. The DTTL (Digital-data Transition Tracking Loop)[1][2][10] bit synchronizer serves as the inner tracking loop of RSS (Range and Synchronization System) [3]. The mean time delay variation in the DTTL is thus an important parameter to be determined when it operates in the channel which causes signal distortion. Based upon the measured data package, the waveforms have been carefully analyzed and modeled[4].

The modeled pulse shapes were used in the simulation to see the time delay variation effect due to speckle-induced waveform distortion and all the measured data were located within two kinds of modeled data set. In this paper, the effect of speckle on the mean time delay variation in the DTTL bit synchronizer is presented based upon the measured data pulses and simulation results. It is known that the worst case delay variation occurs with full DTTL window size (integration interval of quadrature branch) and the mean time delay variation can be mitigated by reducing window size[2][5][6]. To see the effect of window size to the mean time delay variation, the simulation was also performed using window size as a parameter.

In high data rate applications, it is known that analog DTTL, which uses an operational amplifier to implement the integrate and dump circuit, has limit in bandwidth and speed[7]. Therefore, digital implementation was also considered. With the proposed digital DTTL implemen-tation[8], the same simulation was also performed. The difference of the simulation results between analog DTTL and digital DTTL was not so big as expected. Moreover, the simulation results showed the good approximation to the analog case when quantization bit becomes bigger[9]. This paper ends with the conclusion which summarizes the simulation results and suggests further studies to be made.

## Ⅱ. DTTL Overview

For a coherent communication system, several aspects of synchronization such as carrier, subcarrier, frame, word, bit synchronization, etc., are required at the receiver for information recovery. In this paper, emphasis will be put on the bit synchronization and it is assumed that the other synchronizations have already been achieved.

The DTTL is one type of data-derived bit synchronizer which extracts data bits and achieves synchronization directly from the information bearing signal[10]. The presence of adequate transitions (zero crossings) in the data sequence is essential to the success of this type of operation. The DTTL bit synchronizer was first introduced in the high data telemetry receiver of Mariner Mars Mission of 1969. Since then it has become very popular in practical applications. A block diagram of such a loop is given in Fig. 2.1 [1][2][10].

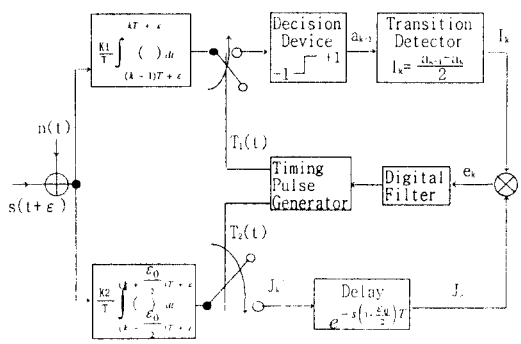



Fig. 2.1 The DTTL (Digital-data Transition Tracking Loop)

The sum of signal plus noise is passed through two parallel branches, which are triggered by a timing pulse generator according to a digitally filtered version of an error signal formed from the product of the branch outputs. Furthermore, the two branches

are held at a fixed phase relationship with one another by the timing generator.

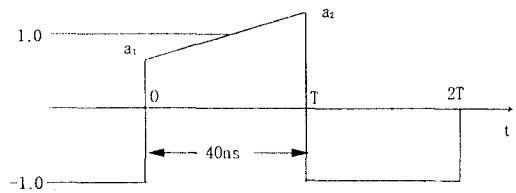
Basically, the in-phase branch monitors the polarity of the actual transitions of the input data and the quadrature branch obtains a measure of the lack of synchronization[10]. The particular way in which these two pieces of information are derived and combined to synchronize the loop is described below. The input signal is passed through in-phase and quadrature integrate and dump circuits. The output of the in-phase integrate and dump is sampled at intervals of T and a ± decision is made corresponding to each input symbol. The transition detector then examines two adjacent decisions $a_{k-1}$, ak and records an input $I_k$ according to the rule in Fig. 2.1.

The output $J_k$ of the quadrature integrate and dump is also sampled at intervals of T and must be delayed before multiplication with the appopriate $I_k$. It is known that an improvement in performance can be obtained by integrating in the quadrature branch only over a portion of the symbol interval (e.g., $[(k+\varepsilon_0/2)T+\varepsilon]-[(k-\varepsilon_0/2)T+\varepsilon]=\varepsilon_0 \quad T;0\le\varepsilon_0\le 1$, where $\varepsilon_0$ is called the window size)[2][5][6]. Then, for proper loop operation, the delay in the quadrature branch must be chosen equal to $(1-\varepsilon_0/2)T$.

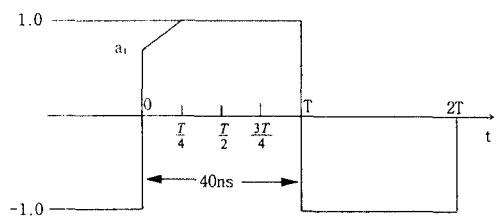
## Ⅲ. Signal Model

For the interest of investigating the effect of signal distortion (due to speckle) on DTTL timing offset variation performance, we isolate the imperfections in hardware implemen-tation and concentrate on the ideal DTTL as depicted in Fig. 2.1. From the data package available, signal distortion is grouped into two different types for simulation convenience[4]. Fig. 3.1 shows the individual signal distortion types. For all types, the negative part of the pulse is assumed to be a perfect rectangle. All distortions occur in the positive part of the signal pulse and the pulse duration T of each part (positive or negative) is 40 ns[5].

Type (a) models the positive pulse to be a linear slope. The slope can be positive or negative depending on the two edge values, $a_1$ and $a_2$. Type (b) models the effect of the various amplitudes of the left pulse edge whose duration is only T/4.




Type (a) Signal Distortion




Type (b) Signal Distortion

Fig. 3.1 Types of signal distortions modeled in simulation

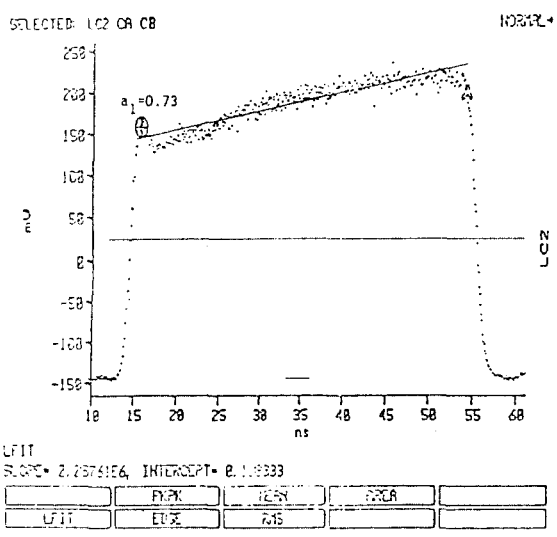



Fig. 3.2 Measured Data of Type (a)

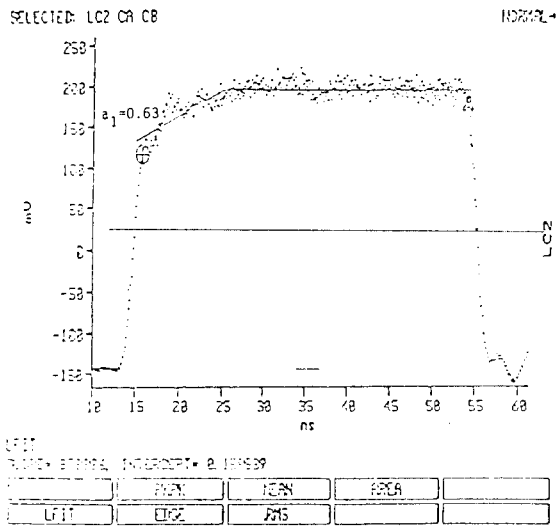



Fig. 3.3 Measured Data of Type (b)

Fig. 3.2 and 3.3 show typical measured waveforms of type (a) and type (b) respectively. Data set #3, #4, #6, #7 which have $a_1 = 1.11$, 0.89, 0.53, 0.73 are matched to type (a); data set #1, #2, #5 which have $a_1 = 0.60$, 0.46, 1.08 to type (b). These data set are used for comparison in the simulation result analysis.

## Ⅳ. Simulation Results

In this section the simulation results are summarized for the different signal distortion types modeled in section 3. Fig. 4.1 shows the DTTL mean time delay variation for type (a) signal distortion. Eleven cases as illustrated in the table on the same page are simulated. The delay in nanoseconds (based on T = 40 ns) is plotted versus the DTTL lower arm integrate and dump circuit window size. The negative value in delay represents the time advance and the delay variation means the variation of delays at the given window size. For example, the delays in case 1 and 11 are −2.5 ns and 2.5 ns, respectively and the maximum delay variation among eleven cases of modeled data set is 5 ns when the window size equals 1.

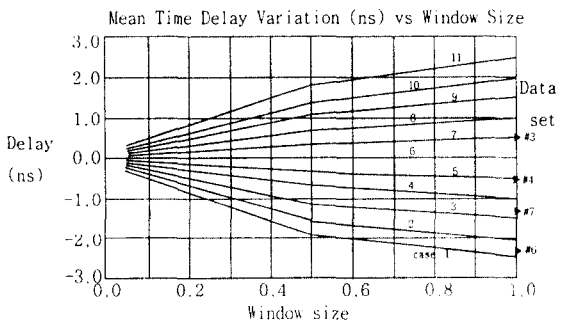
For a fixed window size, the steeper the pulse slope is the larger the absolute value of the steady state delay becomes. For example, the slope of case 1 is steeper than that of case 2 and the resulting delays are −2.5 ns and −2.0 ns, respectively. It is also interesting that signals having the slopes of the same magnitude but of opposite signs have the delays with the same magnitudes but opposite signs. For example, case 2 and 10 have the slopes of the same magnitudes but of opposite signs so that the delays are −2.0 ns and 2.0 ns, respectively, when the window size equals 1.

For a particular case the absolute amount of delay becomes smaller for smaller window size and so the delay variation is[2][5][6]. For this particular signal distortion model a window size of 0.1 yields the maximum delay variation (1 ns which is 2.5% of T = 40 ns) of only about 20% of that (5 ns which is 12.5% of T) for a full window, i.e., window size of 1. On the same plot the data sets obtained are indicated. It can be seen that, for a normalized window size of 1.0, the worst case value is about −2.3 ns (data set #6). The maximum variation among the data set provided is about 2.8 ns which is 7% of T when the window size equals 1 and can be mitigated up to 0.56 ns which is 1.4% of T (between data set #3 and #6).

Fig. 4.2 shows the delay variation performance results for type (b) signal distortion. Delay variation versus aZA is plotted with window size as a parameter. In these cases, for a particular window size we can notice that the delay becomes almost a linear function of the left edge slope $a_1$. The same observation as type (a) signals can be made: 1) the steeper the pulse slope is the larger the absolute value of the steady state delay becomes; 2) signals having the slopes of the same magnitude but of opposite signs have the delays with the same magnitudes but opposite signs for a fixed window size; 3) smaller window size results in smaller delays. For example, case $a_1 = 0.7$ and 0.8 result in the delays of −0.38 and −0.25 ns, and case $a_1 = 0.7$ and 1.3 result in −0.38 and 0.38 ns, respectively, when the window size

equals 1. In this case, the delay variation is 0.76 ns and can be mitigated to 0.24 ns by reducing the window size to 0.1.

The difference is that case $a_1 = 0.5$ gives the maximum delay of $-0.62$ ns compared to the delay of $-2.5$ ns for case 1 of type (a) signals. This result means that type (a) signals introduce more delay variation than type (b) signals. This phenomenon is clear from the fact that type (a) signals are more distorted than type (b) signals. In fact, type (a) signals are roughly four times more distorted than type (b) signals since only a quarter of the pulse duration T in type (b) signals is distorted. It is interesting to see that the resulting delay and its variation of type (a) signals are also roughly four times of those of type (b) signals. For the data sets obtained, the worst case value is $-0.68$ ns (data set #2) and the maximum variation among the data set is about 0.78 ns at the full window and can be mitigated to 0.16 ns with the window size of 0.1 (between data set #2 and #5).




| Case | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| $a_1$ | 0.5 | 0.6 | 0.7 | 0.8 | 0.9 | 1.0 | 1.1 | 1.2 | 1.3 | 1.4 | 1.5 |
| $a_2$ | 1.5 | 1.4 | 1.3 | 1.2 | 1.1 | 1.0 | 0.9 | 0.8 | 0.7 | 0.6 | 0.5 |

Fig 4.1 Mean time delay variation for type (a) signal distortion

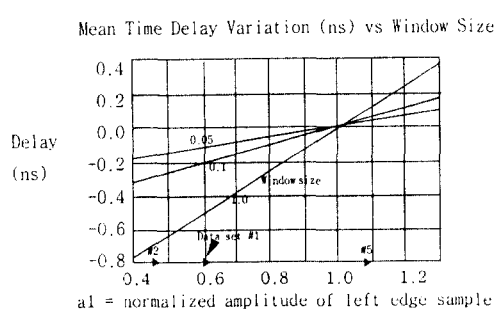



Fig. 4.2 Mean time delay variation for type (b) signal distortion

## V. Digital Implementation

The analog DTTL block diagram shown in Fig. 2. 1 was modified to, what is called, digital DTTL[5][7][8] shown in Fig. 5.1. A front end RC filter followed by an analog to digital converter(A/D) and a subtractor instead of an integrate and dump, are used for high data rate applications. The main reason for the RC filter is that the integrate and dump is usually implemented by using an operational amplifier with feedback and therefore bandwidth limited. It is also difficult to dump (reset) the integrator fast enough at high data rates. The bit synchronizer after the RC filter is implemented by using all digital techniques. The operation principle of the digital DTTL is similar to that of the analog DTTL and is explained well in many literatures[7][8].

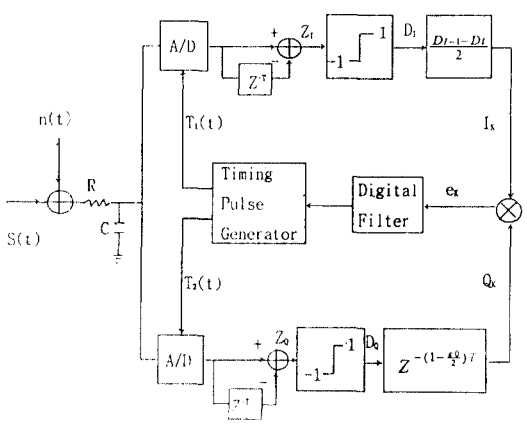



Fig. 5.1 The DTTL with Front-End RC filter

Computer simulation was also done with the digital DTTL bit synchronizer shown in Fig. 5.1 to compare the numerical result of the digital DTTL with that of the analog DTTL and therefore to justify the digital implementation of the given analog DTTL. Only type (a) modeled signal distortions were used in this simulation since type (a) signals have more distortions than type (b) signals. The parameters used in the digital DTTL bit synchronizer simulation are shown in Table 5.1.

Table 5.1 DTTL Simulation Parameters

| | |
|---|---|
| RC filter rise time constant | 50 |
| RC filter fall time constant | 50 |
| Number of A/D quantization bit | 1) 10<br>2) infinity |
| IPM step time | 0.16 ns (256 steps in T) |
| Window size | 0.125 to 1.0 |

The number of bits in A/D and IPM (Incremental Phase Modulator) step time become the critical simulation parameters since both vertical and horizontal values should be expressed in discrete form instead of continuous one in the digital simulation. The number of bits in alalog to digital converter determines the quantization resolution and the IPM step time determines the time resolution. 10 bits of A/D means 1024 discrete values are used to express the measured delay and 0.16 ns of IPM step time means that 256 discrete values in each pulse duration T which is again 40 ns are used to express the discrete time.

Fig. 5.2 shows the simulation result when the number of bits in A/D equals 1) 10 bits with the solid line and dot mark, and 2) no A/D or the case of infinite number of bits with the dashed line and star mark, respectively. Although this simulation was done separately with the analog DTTL simulation, it is interesting to see that the result well-matches to the result of the analog DTTL case. The delays of case #1 and #11 are $-1.98$ ns and 3.11 ns in 10 bits A/D case, and $-2.46$ ns and 2.62 ns in no A/D case, respectively, when the window size equals 1. These values become $-0.39$ and 0.86 ns and $-0.47$ and 0.77 ns, respectively, when the window size reduces to 0.125.

Hence the maximum mean time delay variation is 5.08 ns and 1.24 ns when the window size equals 1 and 0.125, respectively. This result is almost the same as that of analog DTTL (5.0 ns and 1.2 ns, respectively), though the symmetry between positive and negative value does not hold. In fact, we can notice that the maximum variation becomes slightly samller (from 5.09 ns to 5.08 ns when window size equals 1) and delays become more close to the symmetry (from $-1.98\sim+3.11$ ns to $-2.46\sim+2.62$ ns when window size equals 1) as the number of quantization bits goes to infinity from 10 bits.

## Ⅵ. Conclusion

From the results obtained above, it is verified that mitigating the mean time delay variation through reduction of window size is possible. The amount of improvement seems significant. It could achieve a factor of 5 (2.5%*5=12.5% for the modeled data, 1.4 %*5 =7% for the given data) in reduction by reducing window size from 1 to 0.1. However, exact amount of reduction in delay variation epends on particular type of signal distortion.

It is also conjectured that type (a) signal distortion gives much more mean time delay variation than type (b) signal distortion does. Under the same slope and window size, type (b) signal distortion yields a delay variation of only about 25% of that for type (a) signals. This result means that the mean time delay variation performance analysis of DTTL bit synchronizer should be focused on type (a) signal distortion.

From the results shown in Fig. 5.2 we find that as

the number of bits in A/D converter becomes greater than 10 bits and the IPM steps become more than 256 steps, the mean time delay variation performance of the digital DTTL approaches to that of the analog DTTL. This result justifies the practical implementation of the digital DTTL without having a big performance degradation.

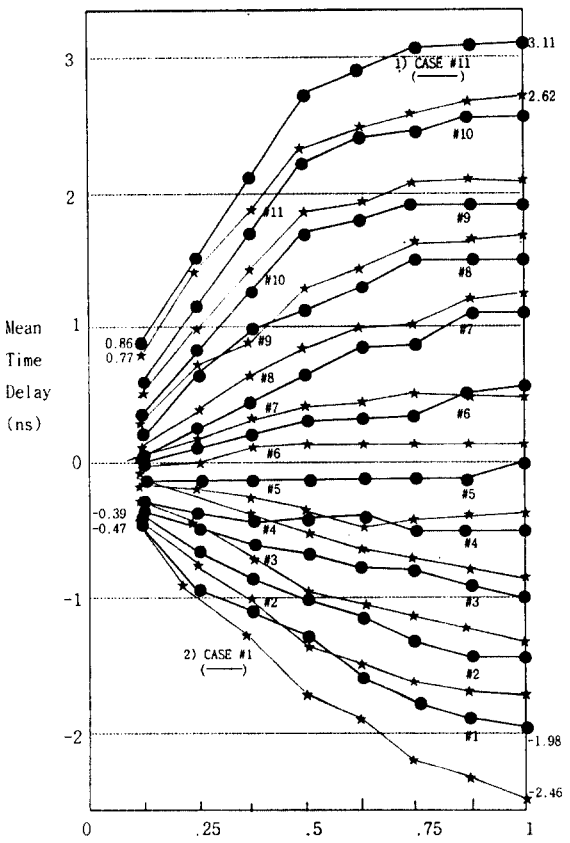



Fig 5.2 Simulation Results for 1) 10 bit A/D (solid and dot) 2) No A/D (dashed and star)

This paper deals only with the mean time delay variation performance of the DTTL circuit due to speckle-induced distortions. Other sources which degrade the performance should be studied further. This paper has also used the well-known mitigation method which reduced the window size. Further efforts are being expended on various mitigation techniques.

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