論文 98-23-3-22

A New Multimedia Delivery System Design using PCI Environment

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PCI 버스를 이용한 멀티미디어 전달 처리 시스템 설계

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ABSTRACT

In this paper, we propose a new multimedia delivery system using PCI (peripheral compliant interface) bus environment. This multimedia delivery system handles multiple MPEG-2 TS (transport stream) packet transmission. This system consists of several media encoding parts and a stream adaptation part connected to PCI bus, and the embedded host processor controls overall system. Video and audio packets is transferred to the stream adaptation parts via PCI interconnection, which has TS processing and ATM network adaptation function. Especially, this multiple TS processor provides multiple multiplexing capability for several audio and video PES (packetized elementary stream) packets. And we show the vacation system modeling and performance analysis for the proposed multiplexing scheme considering PCI packet waiting cycles. The performance analysis shows that the proposed architecture guarantees enough channel capabilities (over 200Mbps). Therefore, this multimedia delivery system can offer simple architecture, effective operation and management scheme, and low cost solution using PC environment.

요 약

본 논문은 복수의 MPEG-2 운송 스트림 패킷 전송을 처리하는 PCI 버스 환경을 이용한 새로운 멀티미디어 전달 시스템에 대하여 제시한다. 제안된 멀티미디어 전달 시스템은 미디어 인코딩 기능과 패킷 스트림 정합 기능으로 구성되며, 내장형 호스트 프로세서에 의해 시스템의 전반적인 운용 및 관리를 담당한다. 비디오 및 오디오 패킷은 PCI 버스를 통하여 MPEG-2 운송 스트림 다중화 처리와 ATM 망 정합을 수행하는 패킷 스트림 정합기능으로 전송되어 가입자에게 분배형 멀티미디어 서비스를 제공한다. 특히, 제안된 MPEG-2 운송 스트림 프로세서는 복수 개의 비디오 및 오디오 PES 패킷의 다중화 처리 기능을 제공한다. 그리고 제안한 멀티미디어 전달 시스템에서의 패킷 다중화 체계는 PCI 버스상에서 Waiting Cycle을 고려한 Vacation 모델링을 제시하며, 성능 분석을 통하여 제안된 시스템 구조가 200Mbps 이상의 처리 대역폭을 제공함을 보여준다. 따라서 제안된 멀티미디어 전달 시스템은 PC 환경의 단순한 구조, 효율적인 운용 및 유지보수 처리, 경제성을 제공함을 보여준다.

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論文番號:97287-0816
接受日字:1997年 8月 16日

Ⅰ. Introduction

Currently, large scale telecommunication providers only offer the distribution services via digital broadcast system, and other information providers also deliver various data services through internet. The advance of access network replaces current service providing scheme with different ways. The concern of subscribers focuses on multimedia interactive services such as home-shopping, video-telephony, VOD, internet access, digital CATV broadcasting service, and so on, through integration of broadcast and telecommunication networks [1][2].

As telecommunication service providers modernize their schemes, their concerns are increasing in upgrading networks to meet not only the near-term requirement of providing high-quality POTS (plain old telephone service) but also the demand for emerging broadband transport services. The access network providers try to merge current and future broadband services, which lead many users to telecommunication networks. Based on advanced infrastructure of telecommunication, the quality improvement and various applications for multimedia services increase the concern for the multimedia content objects in full service network [3].

Figure 1 shows a multimedia distribution scheme using the multimedia delivery system in full service access network [4]. The asymmetry of upstream and downstream bandwidth in a full service access network fits well with current services. For example, in digital video broadcast or video-on-demand service, downstream traffic is a relatively high bandwidth digitally compressed video stream running at a few Mbps. On the other hand, the upstream traffic is usually low bandwidth signaling from user's control such as channel change operation. Future services, such as video telephony or some client-server data communications, will have a more symmetrical requirement for upstream and downstream bandwidth. A full service access network, shown in Figure 1, provides a combination of digital broadcast video, conventional POTS and ATM service, and leased line data services. In case of digital broadcast service using the multimedia delivery system which delivers video and audio stream to ATM networks, broadcast gateway provides the signaling capability to control switched digital broadcasting, establishing ATM connections on behalf of end user and multimedia delivery system. The broadcast gateway maintains all ATM connections, and session and resources used within an interactive session. [5]

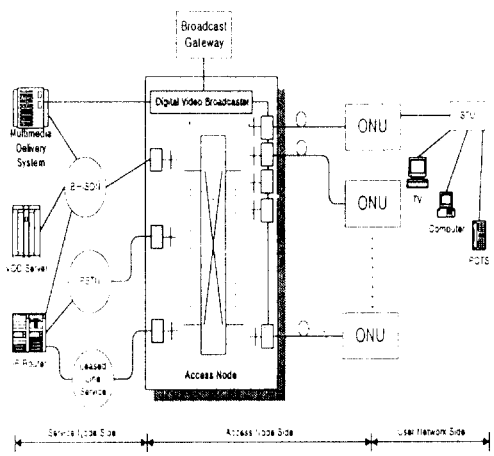

Fig. 1 A multimedia distribution scheme using the multimedia delivery system in full service access network

To offer digital broadcast services, we propose a new multimedia delivery system architecture using PCI bus. The proposed scheme consists of several media encoding parts and a stream adaptation part on PCI bus, and the embedded host processor controls overall system. Video and audio streams are delivered to the stream adaptation part, which has a TS processor and an ATM network adaptation processor. Especially, the proposed multiple TS processor provides multiple multiplexing scheme for several audio and video PES packets through PCI interconnection. The reason using PCI bus is that it can provide real-time full traffics from media encoders to a stream

adaptation. In this paper, we also presents a system modeling for TS packet multiplexing scheme using PCI bus, and the results of performance analysis show that this system architecture guarantees enough channel capabilities for over 10 media encoders. In view point of implementation, this multimedia delivery system can offer simple system structure, effective operation and management scheme, low cost solution, and flexible extendibility under PC environment.

The objective of this paper is twofold. First we introduce a new multimedia delivery system architecture, which meets user requirements for multimedia contents broadcast and delivery over full service network. The proposed system architecture has embedded host processor with PCI bus. Second we also show system performance modeling and analysis for system extension, the optimal transmission size of packetized elementary stream (PES) packets, according to various packet length and media transfer rates under this architecture.

This paper is organized as follows. In section 2 we describe design and architecture of the proposed multimedia delivery system, such as system control scheme, media encoding processor, multiple TS processor, and network adaptation processor. Section 3 shows the system modeling and performance analysis considering several conditions. Section 4 draws conclusions and provides an outlook of how this work will be continued.

Ⅱ. The Multimedia Delivery System Architecture

In this section, we describe the system control architecture, media encoder, TS processor, and ATM network adaptation for the multimedia delivery system. The multimedia delivery system specifications are shown in Table 1.

Table 1. Multimedia Delivery System Specifications for distribution services

Items		Specifications
video	signal format	NTSC, CCIR601
	display size	~ 702×480
	coding format	MPEG-2 MP@ML
	output coding band-width	4~15Mbps
Audio	signal format	Analog(Stereo)
	sampling frequency	32K~48Khz
	coding format	MPEG-1 layer 1, 2
	output coding band-width	192, 256, 384kbps
System	multimedia multplexing	TS level
	network adaptation	AAL5 over ATM
	signalling protocol	Q.2931
	media system control protocol	DSM-CC U-N
	broadcast protocol	Switched Digital Broadcast-Channel Change Protocol

1. System Control Architecture

The embedded host processor controls each media encoder and a stream adaptation (including TS processor and network adaptation processor) through PCI bus. Each media encoder is operated as PCI master mode, and stream adaptation function is driven as PCI slave mode. Figure 2 shows the overall system architecture of the multimedia delivery system.

The host processor performs system operations and controls the overall system through PCI controller of each module. Under operating system supporting multi-tasking, the host processor manages operation mode between PCI master and slave controller, such as initializing PCI controllers, set-up transmission block size, addressing of each receiving target buffers of stream adaptation, and arbitration of PCI bus usage. Second host processor controls media encoders' operation mode, such as system/configuration requirements, operation requirements, media encoder latency, input/output picture mode. Lastly the host processor handles operation mode for stream adaptation, such as set-up and managing for each video, audio, PCR,

PMT, and PAT TS packets, ATM level set-up for ATM network adaptation.

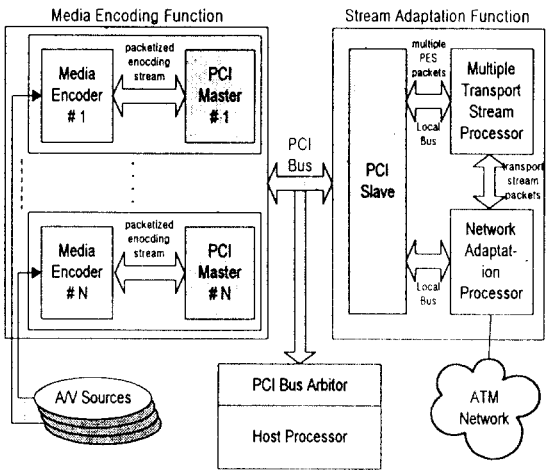

Fig. 2 Overall system architecture of the proposed multimedia delivery system

2. Media Encoding Processor

The media encoding processors encode MPEG-2 video signal and MPEG-1 audio signal, respectively [6].

In case of video processing, MPEG-2 media encoders receive NTSC video signal from outer video source, and change into digital format like YCBCR. The digital YCBCR data and control signal synchronized with 27MHz are transferred to video encoding function. The video encoding function consists of Intra picture processor(I), Forward prediction picture processor(P), and Bi-directional picture processor(B). The encoding processors develop a lower bit rate structure of elementary stream data consisting of, among other things, video sequences, groups of pictures, and single pictures. Although there is a structure within the compressed video elementary stream, it is generally utilized as a single large block or data file. The encoding operation interface allows control of many of encoding parameters, including the ability to compress in I-only mode, IP mode, and full IPB mode. The I, B, P encoding processor transfer video PES packets to a stream adaptation function.

In case of audio processing, audio encoder receives analog audio signals from outer audio source, and after encoding audio data, audio PES packets are also transferred to stream adaptation function concurrently.

3. Multiple Transport Stream Processor

The multiple TS processor multiplexes multiple audio/video PES packets from media encoders, program table packets, and timing packets. TS packets are subparts of PES packets with additional header information. Two important information types of TS packet header are the packet identification (PID), and program clock reference (PCR). Every TS packet has a PID, which is used to reconstruct the variety of separate data streams that may be extant in one TS. PCR is timing information that is used to synchronize the 27-MHz clocks in the encoder and decoder. TS packets are exactly 188 bytes, with a normal header of 4 bytes and a longer header if additional header field is present [7][8].

Audio PES packet length is fixed, but video PES packet length is variable. Video PES packets should be aligned into TS payload unit $N*184$ bytes ($N=1, 2, 3, \ldots$). The TS processor continuously checks each PES packet start codes, on detecting a new PES packet header, the remaining part of current TS payload is added with padding data. The goal of this header check scheme is that the beginning of each media PES packets are aligned into TS payload, and the each media PES packets can be recovered at the receiver successfully.

The proposed block diagram of the multiple TS processor is shown in Figure 3. It extracts each PES packets from PCI slave, then checks the PES packet start codes, if the procedure is correct, sends the TS packets to an ATM network adaptation processor via scrambling function (if it is required) This method executes multiple media packet header generation,

PCR packet, and PSI packet handling for each individual service. The proposed TS processor executes TS packet multiplexing according to its scheduling algorithm and packet's transmission request signals [9] [10].

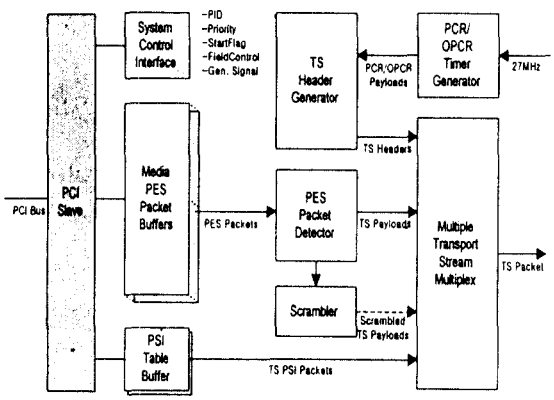

Fig. 3 Block diagram of multiple TS multiplex processor

4. Network Adaptation Processor

Network adaptation processor executes AAL 5 protocol and ATM header processing for TS packets. Signaling processor within host program entity supports network signaling. Network adaptation processor receives two TS packets from upper multiple TS processor at every transmission time. Two TS packet

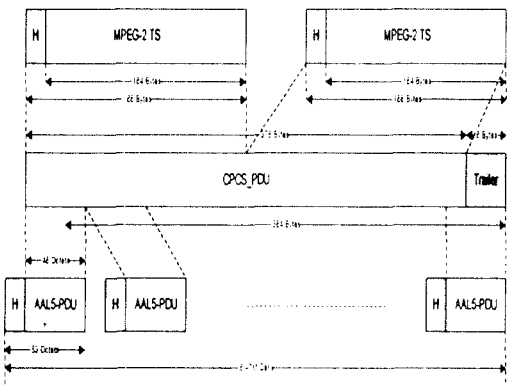

Fig. 4 Network adaptation scheme for 2 single program TS packet

length is 376 bytes, so it well fits to 8 AAL5-PDUs. AAL 5 processor calculates CRC-32 for two TS packets, and the result is attached to 8th AAL5-PDU an AAL5 trailer. In this case, network adaptation processor packetizes 2 single program TS packets that can be either video or any TS packets into single AAL5-PDU. Then the outgoing AAL5-PDU is segmented into 8 ATM cells. After connecting ATM header to each AAL5-PDUs, ATM header processor conveys these cells to ATM network. And the receiver is operated in the reverse way[11]. The network adaptation scheme is shown in Figure 4.

Ⅲ. System Modeling and Performance Analysis

This section presents a multiplex system modeling and system performance analysis for the proposed multimedia delivery system under PCI bus.

1. System Modeling

The PCI bus structure provides peak data transfer rate up to 132 Mbytes/second at 33Mhz. As PCI bandwidth depends primarily on burst length for data transfer, finite bursts will reduce the sustained throughput [12]. In this system, each media encoders can generate the PES packets having various bit rates respectively, so media TS processor can properly schedule the output buffers within media encoders.

It is assumed that each media encoders are normally operated, and the right to access media buffers is given to a media encoder by PCI arbitration logic in a cyclic order. The basic modeling assumptions for PCI operation are as follows:

- Bus arbitration scheme guarantees fairness for PCI bus usage.
- M ($1<M<16$) media encoder operates as DMA master mode, and one media TS processor as DMA slave mode.
- FIFOs are operated with 16bits within PCI master

and slave.

- REQ# signals of M media encoders are all asserted, it is defined as a normal state.

While media encoder#i transfers the PES packet into a target buffer of the media TS processor with DMA operation mode, media encoder#i +1 tries to take PCI bus. After the transaction for bus cycle is occurred, that is, GRANT#i is deasserted, the media encoder#i +1 transfers address and data in the next clock cycle. When a waiting event happens, it causes to lengthen the transaction cycle. Figure 5 shows the basic timing for PCI bus operation with multiple PCI master.

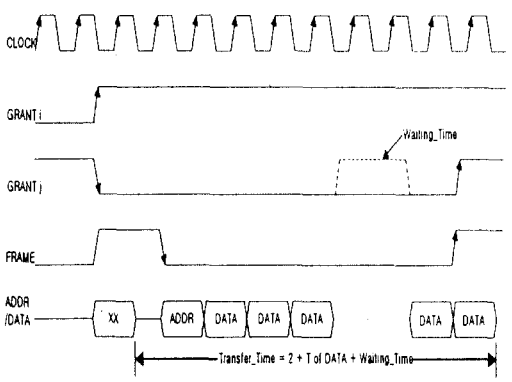

Fig. 5 Basic timing for PCI bus operation with multiple PCI master

2. Performance Analysis

From now on, we analyze the TS multiplex system by using a queueing model, and give some numerical results for our system. Since our system accommodates audio/video packet streams, the delay of packets in the queue(queueing delay) is an important performance measure of our system. So, in the analysis we will derive the PGF of the distribution for the queueing delay and give a numerical result on the change of mean queueing delay with respect to input rates. We will also give a numerical result on the effect of changes for a waiting period on the maximum input rate to be supported by the proposed system.

In analysis we assume the followings:

- Each encoder has an infinite queue and the queue at encoder#i is denoted by "queue i"
- The arrival process at the queue i is according to a renewal process and independent of arrival processes at the other queues. Let r_j^i be the probability that j packets arrive during a clock, and $R_i(z)$ the PGF (Probability Generating Function) of the number of packets arriving during a clock, i.e.,

$$r_j^i \triangleq P\{j \text{ packets arrive during a time clock}\}$$

$$R^{(z)} \triangleq \sum_{j=0}^{\infty} r_j^i \cdot Z^j \tag{1}$$

- Each packet is of fixed size and needs T clocks to be sent, so the service time of a packet is equal to T clock times.
- During each service time, there may occur a waiting event which results in stopping the service, and after a random amount of time the system restarts to serve the remaining payload of the packet which was in service at the occurrence of the waiting event. Let p be the probability that there occurs a waiting event during the service time of a packet, and let fn be the probability that a waiting period, which is defined as the time interval between the occurrence of a waiting event and the service restarting time point, lasts for n time clocks and its PGF is denoted by F(z), i.e.,

$$P \triangleq P\{\text{There occurs a waiting event during a service time}\}$$

$$f_n \triangleq P\{\text{A waiting event lasts for n clocks}\}$$

$$F^{(z)} \triangleq \sum_{j=0}^{\infty} f_j \cdot Z^j$$

- Multiple queues are served in a cyclic order and at each polling instant only one packet of the fixed size is served (if it exists). After completing the service of a queue, say, queue i, the system needs 2 clock times to transfer the address for the queue i +1 before the

queue i +1 is polled, which is captured in our queueing model by introducing a reply time (or switchover time) of fixed length with 2 clock times. When there is no packet to be sent at a polling instant, the system choose the next queue immediately and after a reply time for that queue it serves the queue.

- At each queue, the service discipline is FIFO(first in first out).

To derive the PGF of the queueing delay distribution for packets, we focus on packets arriving at a tagged queue, say queue i. Note that, when a waiting event occurs, the time clocks needed to complete the service of the packet at that time is simply the sum of T clocks (for sending the packet) and the waiting period (whose PGF is given by F(z)). So, the PGF of the total service time of a packet including the waiting period (if any) is given by

$$S(z) = Z^{T[P \cdot F(Z) + (1-P)]} \tag{2}$$

From the above argument we may assume that packet size is variables and its PGF is given by s(z) instead of forgetting the occurrences of waiting events. In addition, the time duration that the system sends packets from queues other than our tagged queue i is regarded as a vacation time. So our tagged queue i is modeled as a GI/GI/1 queue with 1-customer limited service discipline. So, our first step in analysis is to find the PGF $H_i(z)$ of the vacation time. Let Q_j^i be the number of packets in the queue j when the queue i is polled. Denote their joint PGF by $K_i(Z1, ..., Zn)$, i.e,

$$K_i(Z1, ..., Zn) = E\left[\prod_{j=1}^{N} Z_j^{Q_j^i}\right] \tag{3}$$

By the same argument as in Lee[13], $H_i(z)$ is given by

$$H_i(z) = \left[\prod_{j=1}^{N} D_j(z)\right] \cdot \prod_{\substack{j=1 \\ j \neq i}}^{N} \left\{S_j(z) \cdot [1 - K_j(1, ..., 1, 0, 1, ..., 1)] + K_j(1, ..., 1, 0, 1, ..., 1)\right\} \tag{4}$$

where 0 is at the j-th position in the arguments of K_j (1, ..., 1, 0, 1, ..., 1) and

$$K_j(1, ..., 1, 0, 1, ..., 1) = 1 - \frac{2 \cdot N \cdot R_i'(1)}{1 - \left[\sum_{i=1}^{n} S_i'(1) \cdot R_i'(1)\right]},$$

$$(j = 1, ..., N)$$

For details, refer to Lee[13].

Let W_i denote the queueing delay of a newly arriving packet at our tagged queue i and $W_i(z)$ the PGF of the delay distribution for our system. From Lee[13] and the above equations(1), (2), (3), and (4), $W_i(z)$ is given by

$$W_i(z) = \frac{C_i[H_i(Z) - 1][1 - R_i(S(Z) \cdot H_i(Z))]}{R_i'(1)[Z - R_i'(S(z) \cdot H_i(z))][1 - S(z) \cdot H_i(z)]} \tag{5}$$

where

$$C_i = \frac{1 - S'(1) \cdot R_i'(1) - H_i'(1) \cdot R_i(1)}{H_i'(1)}$$

By differentiating $W_i(z)$ in (5) with respect to z and letting z = 1, we obtain the mean delay time $E[W_i]$ for packets in the queue as follows:

$$E[W_i] = \frac{(R_i'(1))^2 \cdot (S''(1) + S'(1))}{2 \cdot R_i'(1) \cdot (1 - R_i'(1) \cdot S'(1) - R_i'(1) \cdot H_i(1)} - \frac{(R_i'(1))^2 \cdot S'(1) \cdot (1 - 2 \cdot H_i(1)) + R_i''(1) \cdot (S'(1) + H_i'(1))}{2 \cdot R_i'(1) \cdot (1 - R_i'(1) \cdot S'(1) - R_i'(1) \cdot H_i(1))} + \frac{(1 - R_i'(1) \cdot S'(1)) \cdot H_i'(1)}{2 \cdot H_i'(1) \cdot (1 - R_i'(1) \cdot S'(1) - R_i'(1) \cdot H_i'(1)}$$

Next, we give some numerical results. For convenience, we assume that the duration of a waiting period is geometrically distributed, but note that our analytic result can be also applied to models where a waiting period has a general distribution. We also assume that there are 10 input queues and the arrival processes at the queues are identical. In figure 6 we give the effect of the change in the input rate on the mean waiting time for a newly arriving packet in the queue. In fig-

ure 6 we assume that the probability p that a waiting event occurs during a service time of a packet is 0.3 and the mean of a waiting period is 1/0.01.

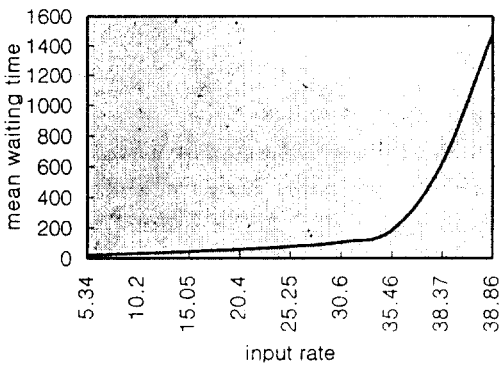

Fig. 6 The change of mean waiting time w.r.t. input rate

In figure 7 we show the maximum input rate to be supported by each encoder when the probability p that a waiting event occurs during a service time of a packet is changed. In figure 7 we assume that the mean of a waiting period is equal to 1/0.01. As one can see in figure 7 the maximum input rate to be supported decreases when the value p increases. The results of performance analysis show that even if probability p reaches to 0.9, this system architecture guarantees enough channel capabilities for over 10 media encoders.

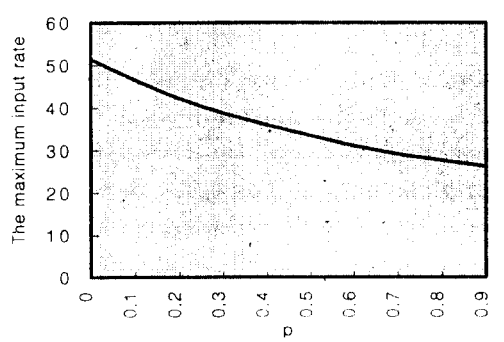

Fig. 7 The maximum input rate w.r.t.p

In figure 8, we give the change of the maximum input rate supported by each encoder with respect to the change of the mean duration of a waiting period. In figure 8 we assume the probability p is equal to 0.3. Figure 7 and 8 show that the changes in the mean duration of a waiting period do not affect the maximum input rate supported by our system more significantly than the changes in p do.

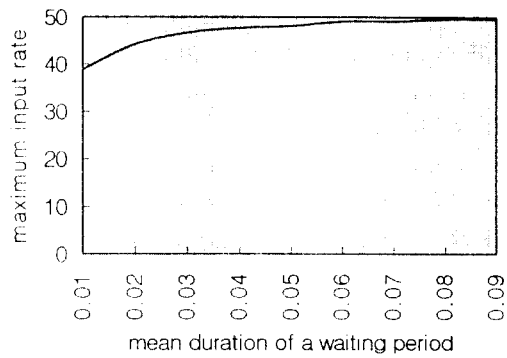

Fig. 8 The maximum input rate w.r.t. mean duration of a waiting period

Ⅳ. Conclusions

In this paper, we proposed a PCI based multimedia delivery system supporting broadcast and distribution services. This multimedia delivery system shows a multiple TS multiplexing scheme through PCI interconnection. The proposed TS processing scheme presented to have multiplexing capability for multiple audio/video PES packets. This structure on PC base offers some advantages, such as simplified scheme for multimedia delivery, system implementation, system control, and so on. The results of performance analysis presented the possible transfer bandwidth and optimal transmission block size without media packet losses, and provided various rate MPEG-2 and HDTV level services as well. For the future works, the next points are added on this scheme with supplementary as follows:

- System structure supporting interactive, retrieval, and On-Demand services.
- System performance analysis considering various bandwidth and VBR services.

Acknowledgment

We would like to thank Dr. Mun-Kee Choi, vice-president, and Dr. Jae-Keun Kim, director of broadband transmission department, for their encouragement and helpful advice. We also appreciate Dr. Gang-Uk Hwang for system modeling guidance.

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