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Error Control Architecture for ATM Data Transmission over Wireless Links

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ABSTRACT

In this paper we describe our investigation on ATM over wireless links, where focus on the impact of the bit error characteristics of a wireless link on ATM. We first analyze the ATM header error correction (HEC) mechanism and calculate ATM Quality of Service(QoS) parameters such as the cell loss ratio(CLR), the cell error rate(CER) for a wireless link. In the second part of the paper we suggest possible error control scheme to improve performance degradation caused by burst errors. Especially this paper provides performance comparison between concatenated FEC and type I hybrid ARQ through the use of packet error rate and throughput. Finally we recommend error control architecture for ATM data transmission over wireless links.

I. Introduction

Asynchronous transfer mode (ATM) technology will have an important role in the future evolution of global communication networks. ATM is a transmission procedure based upon asynchronous time division multiplexing procedure using 53 bytes cell. while ATM results in considerable advantages (less overhead, increased throughput) in an optical network, it also causes severe problems when ATM data is transmitted over an error-prone channel, wireless channel as shown in Fig. 1(1). A terrestrial wireless channel can be approximated as an Rayleigh fading channel. Such a channel produces random bit errors, and the error rate depends on the received signal-to-noise ratio, which for digital communications can be expressed as the ratio of the bit energy to the noise spectral density, E_b/N_o. Wireless systems are power limited and Forward Error Correcting(FEC) codes are used to guarantee reliable transmission even at very low signal to noise ratios. However, when a decision error occurs, a large number of bits is affected(e.g. ten to forty bits, depending on the code), resulting in burst errors. Because ATM was designed to be robust with respect to random signal bit errors, burst error considerably degrade the performance of ATM. This paper is structured as follows. The impact of burst and random errors on the ATM layer is analyzed in section 2.

Error control scheme that include the concatenated FEC and type I hybrid ARQ is considered and analyzed to improve wireless link performance in section 3. Performance of error control schemes is also compared in section 3. In section 4 recommended error control architecture is given with tradeoffs for delay-sensitive traffic and for nondelay-sensitive traffic, and the paper closes with a remark.

II. QoS Parameters on the ATM Layer

We analyze the ATM header error correction (HEC) mechanism and calculate ATM Quality of Service(QoS) parameters such as the cell loss ratio(CLR), the cell error rate(CER) for a wireless link(2,3). We thereby focus on the impact of bit error characteristics on the ATM layer with two different types of error events (random single bit errors and burst errors).

2.1 Performance model for random single bit errors

We assume that independent and identically distri-

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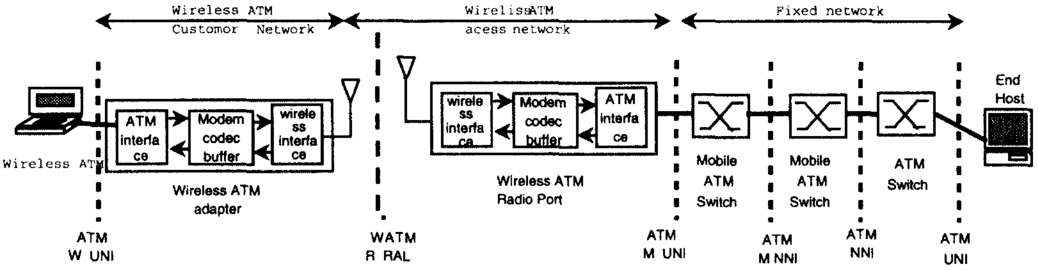
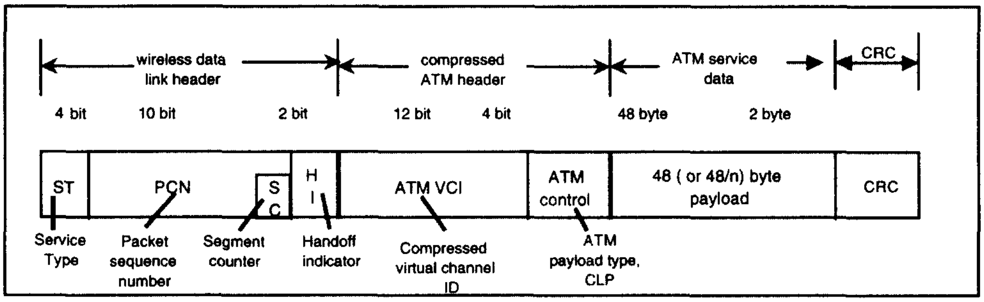


(a) Reference configuration



(b) Wireless ATM cell

Fig. 1 The reference configuration of wireless ATM network

buted random single bit errors occur on the transmission link at a given bit error rate(BER) p. To compute the interesting QoS parameters, we have to find the probability that there are n bit errors in a block of length h, which is given by the binomial distribution. The subscript s was used to denote single random bit errors.

$$P_s(n) = {}_hC_n\, p^n(1-p)^{h\quad n} \qquad (1)$$

CLR (Cell Loss Ratio) is the probability that a cell is discarded. The ATM cell header is protected by a code that can correct single bit errors. If no other means would have been taken, the CLR could simply be computed as the probability that more than one error occurs, which is equal to $1-P_s(0)-P_s(1)$. However, to reduce the vulnerability to burst errors, a dual mode operation of the HEC was chosen.

Hence, the cell loss ratio equals CLR = P(correction mode) • P(>1 error in header) + P(detection mode) • P(≥1 error in header) = $P_c\,[1-P_s(0)-P_s(1)]+P_d\,[1-P_s(0)]$. Pc and Pd are the probabilities that the receiver is in correction mode and in detection mode, respectively. These two probabilities can be computed by modeling the dual mode operation of the HEC mechanism as a Markov chain with two states. Solving the state equations yields $P_c = P_s(0)$ and $P_d = 1-P_s(0)$. In this case *h* is 16, the number of compressed ATM header bits shown in Fig. 1.

$$\begin{aligned} CLR &= P_s(0)[1-P_s(0)-P_s(1)]+[1-P_s(0)][1-P_s(0)] \\ &= 1-P_s(0)-P_s(0)\,P_s(1) \qquad (2) \end{aligned}$$

CER is defined as the ratio of errored cells to the number of totally delivered cells. Errored cells are cells with at least one error in the payload. The probability that one or more random bit errors hit a payload can be derived from (3) and i = 384 is the number of information bits in the ATM payload.

$$CER = 1-(1-p)^i = 1-P_s(0) \qquad (3)$$

2.2 Performance model for burst errors

Assuming that both error bursts and errors in a burst are Poisson distributed, we get the Neyman-A contagious model. In this case, $P_B(n)$ is the probability that n errors occur in an interval of h bits when the mean error burst length is b and p denotes the bit error rate at the output of decoder. The subscript B denotes burst errors.

$$P_B(n)=\frac{b^n}{n!}\exp\left(\frac{-hp}{b}\right)\sum_{j=0}^{\infty}\left(\frac{hp}{b}\exp(-b)\right)^j\frac{j^n}{n!} \quad (4)$$

Since we are only interested in a rough approximation, CLR is modelled as the probability that more than one error occurs, neglecting the fact that ATM actually uses a dual mode operation for the HEC and neglecting undetected errors. In this case h is 16, the number of compressed ATM header bits shown in Fig. 1.

$$\begin{aligned} CLR &= 1-P_B(0)-P_B(1) \\ &= 1-\exp\left(-\frac{16p}{b}\right)\left[1+\frac{(1+b)16p}{b}\exp(-b)\right] \end{aligned} \quad (5)$$

CER is computed as the probability that one or more errors occur in the information field of the ATM cell, using the same model as used in computing CLR. In this case, h is 384, the number of payload bits.

$$CER = 1-P_B(0) = 1-\frac{\exp\left(-\frac{384p}{b}\right)}{1-\frac{384p}{b}\exp(-b)} \quad (6)$$

2.3 Performance analysis

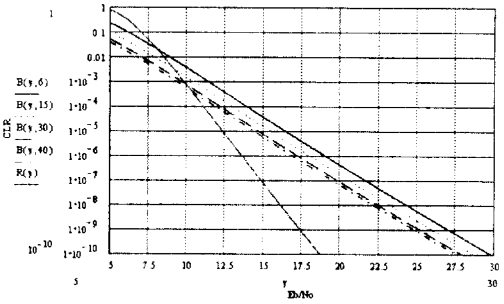
To analyze wireless link performance, we assume binomial distribution for random single bit errors, and assume Poisson distribution for burst errors. A FEC code with a constraint length 7 rate 1/2 is used and a QPSK is used as modulation scheme. The relation of p, p_e and γ is shown in (7). p_e denotes the bit error rate at the output of demodulator and γ is the ratio of the bit energy to the noise spectral density (Eb/No) at the input of demodulator.

$$p(M=4) \le 1/2(7D^7+39D^8+104D^9+352D^{10}) \quad (7)$$

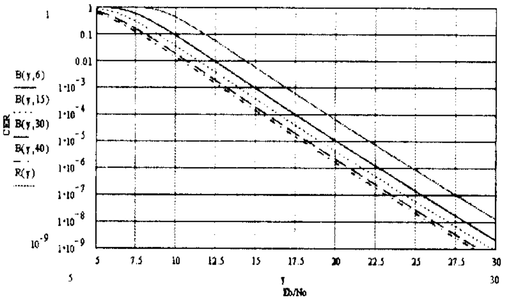
$$D = 2\sqrt{\frac{p_e(1-p_e)}{M-1}}+\left[\frac{M-2}{M-1}\right]p_e$$

$$p_e=\frac{1}{2}\left[1-\frac{1}{\sqrt{1+\frac{848}{424\gamma}}}\right]$$

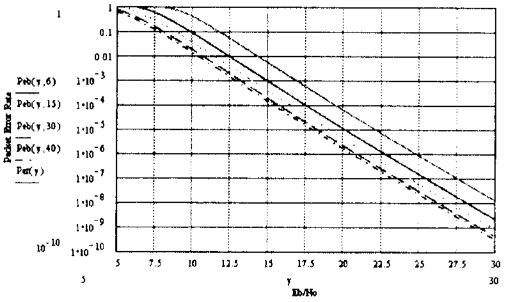
The theoretical results are shown in Fig. 2. B(γ, b) represents CLR or CER for b = 6,15,30,40 burst errors.



(a) CLR



(b) CER



(c) PER

Fig. 2 Curve for CLR, CER, PER in terms of the Eb/No

R(γ) represents CLR or CER for single random bit error. We also define PER(Packet Error Rate) as the summation of CLR and CER. Peb(γ, b) represents PER for b = 6,15,30,40 burst errors. Per(γ) represents PER for single random bit error.

Comparing the ATM QoS parameters for random single bit errors and burst errors, it can be seen that the CLR degrades on a link with burst errors, whereas the CER and PER actually improve on a link with burst errors. This is due to the fact that for a given Eb/No a burst of length b usually destroys only a single cell, whereas b random single bit errors would affect b cells. Generally, it is superior for random single bit errors(fiber) than for burst errors(wireless link). The underlying reason for the poor performance of the ATM HEC code is that on a wireless link an undesired concatenation of the convolutional channel code and the ATM HEC code takes place. Therefore, a better improvement should be achieved by using additional scheme on the wireless link to protect the ATM cells.

III. Error Control Schemes and Performance Analysis

The purpose of this section is to investigate error control issues encountered in using ATM over wireless data links. These results will show that ATM can be made to perform satisfactorily over wireless data links if certain error control measures are used to insure that RF link characteristics do not impair ATM operation.

Table 1. Performance improvement schemes

layer	performance improvement scheme
ATM layer	-
DLC sublayer	ARQ
MAC sublayer	-
TC sublayer	multiple access, FEC, interleaving
PMD sublayer	sector antenna, diversity, equalization

We will provide recommendations for improving overall performance using forward error correction(FEC) and data link layer automatic repeat request (ARQ). Especially this section provides performance comparison between FEC and ARQ through the use of packet error rate and throughput. To analyze performance improvement, we use a Rayleigh fading channel and QPSK modulation scheme. Wireless ATM cell format for performance analysis of error control schemes is shown in Fig. 1. The length of wireless ATM cell is 54 bytes, 48 bytes for payload, 2 bytes for compressed ATM header, 2 bytes for wireless data link header, 2 bytes for CRC[1]. Packet is defined as the compressed ATM header and payload, 50 bytes. Packet error rate is defined as the ratio of errored or discarded packets to the number of totally delivered packets and throughput is defined as the ratio of payload bit length of successfully delivered packet to totally delivered bit length.

3.1 Concatenated FEC scheme

Convolutional code(code rate r = 1/2, constraint length $\nu = 7$) is used as inner code, truncated BCH code(n, k, d) is used as outer code. Packet error rate of concatenated FEC scheme is shown in (8) and throughput is shown in (9).

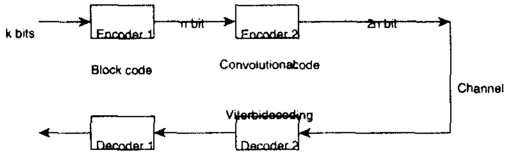


Fig. 3 Concatenated FEC scheme

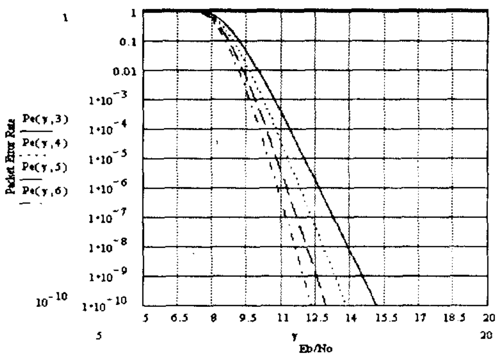
$$P_e(\gamma,t) \le 1 - \left[\sum_{i=0}^{t} \binom{n}{i} (1-p_e)^{n-i} p_e^i \right] \tag{8}$$

$$\begin{aligned} \eta(\gamma,t) &= \frac{k'}{n'} (1 - P_e(\gamma,t)) = \frac{k'}{n'} \left[\sum_{i=0}^{t} \binom{n}{i} (1-p_e)^{n-i} p_e^i \right] \\ &= \frac{k'}{n'} \left[\sum_{i=0}^{t} \binom{400+9t}{i} (1-p_e)^{400+9t-i} p_e^i \right] \end{aligned} \tag{9}$$

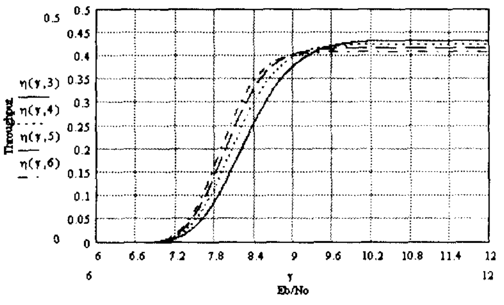
p_e is bit error rate after convolutional decoding as $p_e \le 1/2(7D^7 + 39D^8 + 104D^9 + 352D^{10})$, D is Bhattachayya upper limit as $D = 2\sqrt{\frac{p(1-p)}{M-1}} + \left[\frac{M-2}{M-1}\right]p$ and p is bit error rate at the output of demodulator as $p = \frac{1}{2}\left[1 - \frac{1}{\sqrt{1+\frac{2n}{k\gamma}}}\right]$. k' is 384 bit as the length of ATM payload, k is 400 bit($k'+16$ bit) as the length of payload and compressed ATM header. and n is $400+9t$ bit(data length after outer coding), n' is $2n+32$ bit(wireless ATM cell length after inner coding). Performance result of concatenated FEC scheme is shown in Fig. 4. Packet error rate and throughput are represented as Pe(γ, t) and $\eta(\gamma, t)$ for error correction capability t = 3,4,5,6, respectively.

3.2 Hybrid Type-I ARQ scheme(SR ARQ+FEC/ED)

The type-I hybrid-ARQ protocol is the simplest of the hybrid protocols. Each packet is encoded for both error detection and error correction. These protocols can be implemented using either one-code or two-code systems. Packet error rate and throughput are shown in (10) and (11). Performance results of two code system are shown in Fig. 5

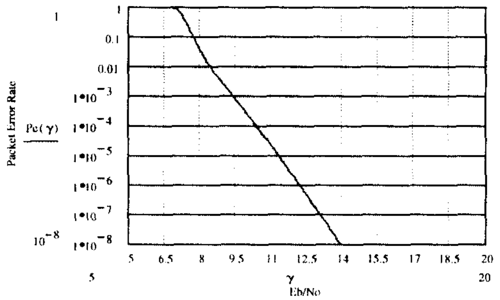


(a) Packet error rate

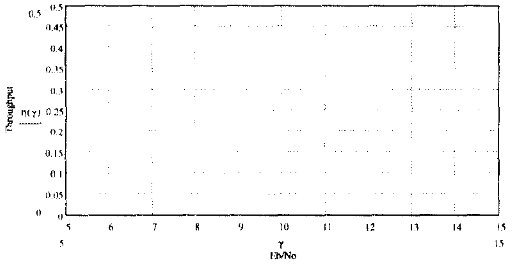


(b) Throughput

Fig. 4 Performance of concatenated FEC code system



(a) Packet error rate



(b) Throughput

Fig. 5 Type I hybrid ARQ scheme(two code system)

$$P_e(\gamma) = \frac{P_{de}P_e}{1 - P_{de}P_r} \tag{10}$$

$$\eta(\gamma) = \left(\frac{k'}{n'}\right)(1 - P_r P_{de}) \tag{11}$$

P_e is the probability that a received packet contains an undetectable error pattern and satisfies the equation $P_e \le 2^{-(n_1-k)}[1+(1-2p_{be})^{n_1} - 2(1-p_{be})^{n_1}]$. P_r is the probability that a received packet contains a detectable error pattern and thus causes the generation of a retransmission request, satisfies the equation $P_r = 1 - P_c - P_e$. P_c is the probability that a received packet is error-free and satisfies the equation $P_c \ge (1-p_{be})^{n_1}$. p_{be} is the bit error rate at the output of viterbi decoder and satisfies the equation $p_{be}(M=4) \leq 1/2(7D^7+39D^8+104D^9+352D^{10})$, $D = 2\sqrt{\frac{p(1-p)}{M-1}} + \left[\frac{M-2}{M-1}\right]p^{(4,5)}$. p is the channel bit error rate as $p=\frac{1}{2}\left[1-\frac{1}{\sqrt{1+\frac{n_2}{k\gamma}}}\right]$. P_{de} is the probability of FEC decoder error and satisfies $P_{de} \leq 1-P_c$. n_1 is the total length of error detection code(400 bit+9 bit), n_2 is the total length of FEC code(code rate = 1/2, constraint length = 7, length = 409 bit+409 bit). k is the information bit length(400 bit), n' is the length of wireless ATM cell after coding (432 bit+9 bit+409 bit) and k' is the payload length of ATM cell(384 bit). Originally P_{de} *is* $\sum_{j=d_{\min}}^{n_2} A_j \sum_{k=0}^{\frac{d_{\min}-1}{2}} P_l^j$, which P_l^j *is* $\sum_{r=0}^{l} {}_jC_{(l-r)}\ {}_{(n_2-j)}C_r\, p^{j-l+2r}(1-p)^{n_2-j+l-2r}$. Pe *is* $\sum_{j=dmin}^{n_1} A_j\, p^j(1-p)^{n_1-j}$, and P_c *is* $\sum_{j=0}^{\frac{d_{\min}-1}{2}} {}_{n_2}C_j\, p^j(1-p)^{n_2-j}$.

Type I hybrid ARQ scheme use an error-control code of fixed rate for error-correction in each transmitted packet. In such scheme, the code rate must be carefully chosen to match the channel bit error rate in order to maximize throughput. Whenever there is a mismatch between code rate and channel BER, the throughput suffers. To compensate this demerits, adaptive type I hybrid ARQ scheme estimates the channel BER in real time, and based on this channel state information, selects the best code rate to use in order to achieve the maximum throughput. Adaptive type I hybrid ARQ scheme uses two codes C_1 and C_2. The code C_1 is a high rate(n, k) block code used for error-detection, and the code C_2 is a rate $R=(b-1)/b$, $b>1$, punctured convolutional code of memory order ν used for error-correction with Viterbi decoding.

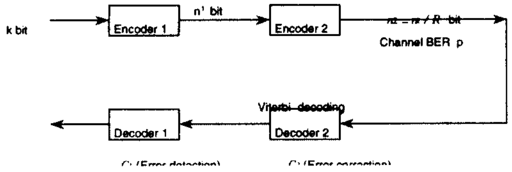


Fig. 6 type I hybrid ARQ scheme

The probability that a received packet will be accepted by the receiver and delivered to the user is then $P=P_c+P_e$. P_c denotes the probability of error-free decoding, P_e denotes the probability of undetected errors. With appropriate selection of the error-detection code C_1, the probability of undetected error P_e can be assumed to be negligible and P is approximately P_c. When P_{be} is the probability of an error event of Viterbi decoding, the probability of error-free decoding P_c may be lower bounded as $P_c \geq [1-P_{be}]^{n_1}$, which satisfies $P_{be} \leq \sum_{d=d_{free}}^{\infty} a_d P(d)$ where d_{free} and a_d are the free distance and the weight spectra, of the code C_2, respectively, and where $P(d)$ is given by (13)[4]. The throughput of the type I hybrid ARQ system with selective-repeat protocol is given by (12). The error-detection code C_1 has 9 parity-check bits and the code C_2 are the punctured convolutional codes produced from the rate 1/2 convolutional code of memory order $\nu=7$. The code rate R of C_2 varies from 1/2 to 7/8 and the packet length is $k=400$.

$$\begin{aligned}\eta &= \frac{\textit{the average information bits}}{\textit{transmitted channel bits}} = \frac{k'}{n'}(1-P_rP_{de}) \\ &= \frac{k'}{\frac{n_1}{R}+32}(1-P_rP_{de}) \\ &= \frac{384R}{409+32R}(1-P_rP_{de}) \\ &= \frac{384R}{409+32R}[1-(1-P_c-P_e)(1-P_c)]\end{aligned} \tag{12}$$

where $P_e \leq 2^{-(n_1-k)}[1+(1-2P_{be})^{n_1}-2(1-P_{be})^{n_1}]$, $p=\frac{1}{2}\left[1-\frac{1}{\sqrt{1+\frac{n_1/R}{k\gamma}}}\right]$, $P_r=1-P_e-P_c$, $P_{de} \leq 1-P_c$ is used. k' is 384 bit, k is 400 bit, ν is 7, n_1 is $k+9$, R is code rate of convolutional code (7/8, 6/7, 5/6, 4/5, 3/4, 2/3, 1/2), n_2 is n_1/R, n' is n_2+32. Throughput is shown in Fig. 7.

$$P(d) = \sum_{j=\frac{d+1}{2}}^{d} \binom{d}{j} p^j(1-p)^{d-j} \quad (d: odd) \tag{13a}$$

$$\sum_{j=\frac{d}{2}+1}^{d}\binom{d}{j}p^{j}(1-p)^{d-j}+\frac{1}{2}\binom{d}{d/2}(p(1-p))^{d/2}\quad(d:even) \tag{13b}$$

From Fig. 7 we observe as the channel Eb/No increases the throughput increases for systems with R. However, throughput can be improved considerably by switching to the next system with higher rate R at clearly defined crossover points. The overall maximum achievable throughput is then the envelope of the curves in Fig. 7. Throughput of adaptive type-I hybrid ARQ scheme with different code rate is represented as $\eta n(\gamma, n/(n+1))$ for n = 1,2,3,4,5,6,7 with code rate n/(n + 1).

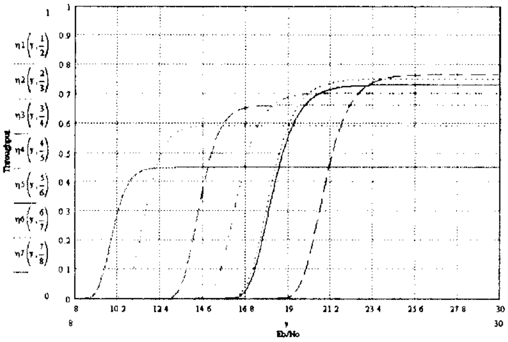


Fig. 7 Throughput of adaptive hybrid type-I ARQ scheme

3.3 Performance comparison

Packet error rate after error control scheme is applied is better than that before. For example, for γ = 15 dB packet error rate before applying error control scheme is $9.731*10^{4}$, $5.609*10^{3}$, respectively in case of burst errors(b = 6) and single bit error. Whereas packet error rate of concatenated FEC(t = 3) and type I hybrid ARQ scheme is $1.757*10^{10}$, $5.403*10^{10}$ respectively. Throughput of concatenated FEC(t = 3) and type I hybrid ARQ scheme is 0.433, 0.452, respectively. Type I hybrid ARQ scheme use an error control code of fixed rate for error-correction in each transmitted packet. Whenever there is a mismatch between code rate and channel BER, the throughput suffers. The code rate can be chosen to match the channel bit error rate in order to maximize system throughput. This scheme, what is called, adaptive type I hybrid ARQ scheme operates in one of several possible states based on the channel BER. When the channel BER increases, the scheme generates additional parity bits for error correction.

IV. Recommended Error Control Architecture

There are a number of tradeoffs that can be made in optimizing performance. Since the wireless environment can vary widely, the choices made will be strongly influenced by the wireless channel characteristics. Therefore, there will be variations in the appropriate choices of parameters for different channels. Several variations on this architecture may be more suitable depending upon channel conditions. Interleaver/deinterleaver is needed only for burst noise channels. This interleaver is not needed for channels which have not significant burst noise problem. The best choice of interleaver for traffic requiring reliable delivery may be too long for delay sensitive traffic. The solution for this situation is to introduce the mux/demux function. This will allow delay sensitive traffic to have a different interleaver length and a different FEC approach if desired. Thus, delay sensitive traffic can use a shorter interleaver length to keep the delay small, and the rest of the traffic can use a longer interleaver to minimize BER. In conclusion, delay critical service make use of a concatenated code which consists of block code and convolutional code. Therefore, CBR service make use of FEC scheme, which its reliability

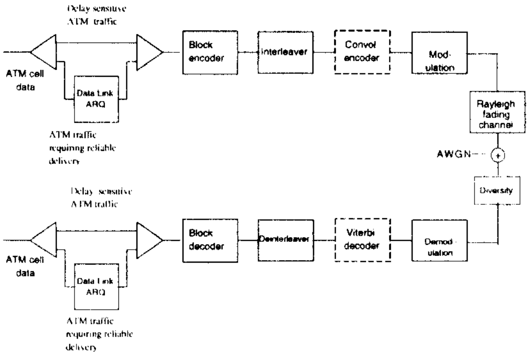


Fig. 8 Error control architecture to improve wireless ATM network performance

drops with the channel quality. For communications which require high reliability, ARQ is needed, but FEC cab be used to reduce the number of retransmissions, known as hybrid ARQ scheme.

V. Remarks

We recommend that it is very important to attempt to make the physical link be SONET-like on wireless channels. Convolutional coding with viterbi decoding is very widely used on wireless communication links. However, a concatenated coding scheme using the outer BCH code and an inner convolutional code provides much better performance. We also recommend that a ARQ protocol be utilized for all traffic requiring reliable delivery. In conclusion, an error control mechanism for improving the quality of wireless links makes them closer to fiber link quality. The specific measures chosen will be influenced by the type of wireless link and its intended usage. For example, satellite and terrestrial wireless links have different characteristics and will require different optimization of the error control mechanisms and parameters within this error control schemes.

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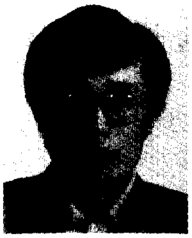

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