시간지연 및 전력지연 프로화일형의 역방향 CDMA PCS 시스템에 미치는 영향

정회원 정 연 호*

Impact of the Time Dispersion and Power Delay Profile Shape on the Performance of a Reverse Link CDMA PCS System

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ABSTRACT

This paper presents the impact of time dispersion and power delay profile shape on the performance of a reverse link direct sequence code division multiple access (DS/CDMA) system. A reverse link CDMA PCS simulator has been developed to observe the performance variation with respect to the time dispersion and power delay profile (PDP) shape. That is, time dispersion, the length and average attenuation of the main profile (the first 3 echoes) and the average attenuation of the second echo group have been considered. A total of 80 PDPs were applied to the simulator and the results show that unlike a TDMA-based system (e.g. GSM), delay spread does not show a good correlation with the performance. In fact, average delay is found to have better correlation with the system performance in a CDMA PCS system. In addition, among the factors related to the PDP shape, the performance appears more sensitive to the relative power level of the main profile.

I. Introduction

Due to increasing demand on mobile radio services, a PCS system has been deployed in many countries and it is based on a microcell structure. A CDMA PCS system is regarded as a wideband system because the transmission bandwidth is much greater than the coherence bandwidth. It has been known that the performance of wideband mobile radio systems varies greatly, dependent upon the degree of time dispersion as well as other channel impairment factors[1-4]. It is, therefore, important to analyze the performance in relation to conceivable channel conditions. In general, the frequency selectivity dominant in wideband systems causes the ISI. Thus, an adaptive channel equaliser is usually required for an acceptable performance as in GSM-based systems[1,5]. In the CDMA PCS system, however, there is a Rake receiver in place of an equalizer. The role of a Rake receiver is considered to be important because the Rake receiver exploits the wideband characteristics for improving the system performance in the DS/CDMA system. The method used in the Rake receiver is often called frequency diversity.[1]

The reverse link CDMA PCS system is chosen for the investigation of the impact of time dispersion and PDP shape on the performance. In performing this investigation, there could be three methods; theoretical considerations, field trials and software simulation. The first two methods would involve either complicated mathematical study or

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[1] It can also be viewed as path diversity, because the Rake receiver operates with individual paths whose statistical characteristics are independent

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a large number of measurements. Hence, those methods are time-consuming and costly. The method of software simulation provides a great deal of flexibility, repeatability and ease of use. The present study has used the CDMA PCS simulator developed for the investigation and an extensive number of channel environments represented by power delay profiles have been applied to evaluate how the performance varies in terms of the time dispersion and power delay profile shape. In the following section, the wideband mobile radio channel is described, followed by the description of the simulator of a CDMA PCS system (upbanded IS-95). Simulation results and conclusions are presented in the subsequent section.

Ⅱ. Wideband Mobile Radio Channel

The real mobile radio channel can be regarded as a WSSUS channel and its properties can therefore be expressed completely in terms of a power delay profile2). From a power delay profile, a number of wideband channel parameters, such as average delay, delay spread, delay interval and delay window can be extracted. These parameters are defined as follows.

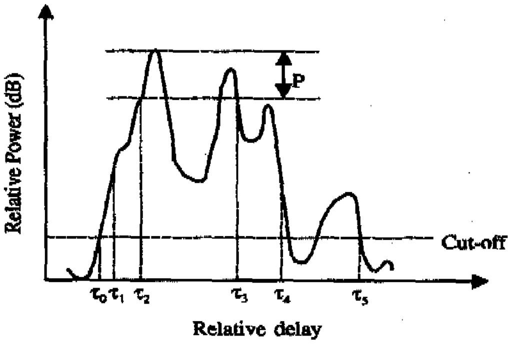

Fig. 1 Example of a power delay profile

An example of power delay profiles is shown in Figure 1. From this figure, the average delay D is the first central moment as defined in Eq.(1).

$$D=\frac{\int_0^\infty \tau P_h(\tau)d\tau}{\int_0^\infty P_h(\tau)d\tau} \tag{1}$$

The delay spread is the square root of the second central moment defined as Eq.(2).

$$S=\sqrt{\frac{\int_0^\infty (\tau-D)^2 P_h(\tau)d\tau}{\int_0^\infty P_h(\tau)d\tau}} \tag{2}$$

The delay interval is defined as the difference in time delay between the point where for the first time the power delay profile crosses a given threshold, (say *P*) and the point where it passes that threshold for the last time. From Figure 1, it is defined as

$$I_p=(\tau_3-\tau_2)_p \tag{3}$$

The delay window represents the duration of the middle portion of the power delay profile containing a specified percentage (*q* %) of the total energy. It is defined as

$$W_q=(\tau_4-\tau_1)_q \tag{4}$$

Depending upon the threshold value (*P*) for the delay interval, there could be many delay interval values. However, delay intervals at 5 dB, 10 dB and 15 dB are often used. Likewise, delay window at 90%, 75% and 50% are usually selected.

In connection with these wideband channel parameters, it should be noted that the values of delay interval and delay window actually measured will vary, depending upon the channel impulse measurement system being used. The values of these parameters produced by a channel sounder having a certain time resolution may differ from those obtained from another channel sounder with a different time resolution capability. The range of the variation of these values is also related to the mobile radio environment where the measurement is conducted.

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2) It should be noted that the term *power delay profile* actually means average power delay profile.

Ⅲ. CDMA PCS System

The simulator of a reverse link CDMA PCS system (data rate of 9.6 kbps) has been developed on Ptolemy simulation platform[6] with conformance to the CDMA PCS specifications[7]. Figure 2 shows the block diagram. The simulator consists of a number of blocks (called 'star' in the Ptolemy terminology). The brief functionality of the main blocks is described below.

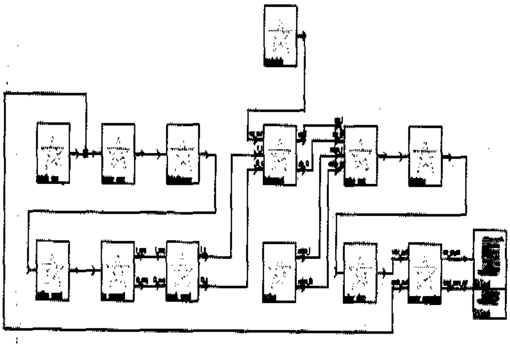

Figure 2. Block diagram of the CDMA PCS simulator

The speech source block contains the speech data (172 bits) obtained from a PRBS generator. It also includes the frame quality indicator (12bits) as well as the convolutional encoder tail (8 zero bits). The convolutional encoder has a rate of 1/3 and the constraint length is 9. The data rate of 9.6 kbps has 100% duty cycle (i.e. continuous) and thus there is no symbol repetition. The interleaving process chosen in the CDMA PCS system is block interleaving using a 32 x 18 array. The next block performs a 64-ary orthogonal modulation. The reason for the use of orthogonal modulation is that for M 8 in M-ary modulation, the orthogonal modulation performs better than DPRK[8]. For orthogonal modulation, the Walsh code is used and this code has an excellent cross-correlation property. The Walsh code is orthogonal for the period of 64 T_c, where Tc is chip period. The modulation process is performed with 6 coded symbols obtained from the output of interleaver block. That is, the coded symbols uniquely identify one Walsh waveform among 64 possible waveforms by using the modulation symbol index. The orthogonally modulated symbols are then spread by long code whose period is $2^{42}-1$. This process is needed for scrambling of the user data and privacy. The I- and Q-channel data are separately spread by the I- and Q-channel PN codes (also called short codes) whose period is 2^{15}. The Q-channel data are delayed for a half-chip period (406.9 ns) before the PN code spreading, thus performing offset QPSK (OQPSK) modulation. After baseband filtering, the I- and Q- channel data modulate the carrier signals ($\sin \omega_c t$ and $\cos \omega_c t$) followed by phase mapping.

In order to simulate the behaviour of the mobile radio channel, an appropriate channel model that incorporates channel impairments (e.g. fading, time dispersion and Doppler shift) is required. A wideband channel model is represented using a tapped delay line model whose details are described in the literature[4].

In the PCS system, the receiver has a Rake structure and the noncoherent demodulation in the reverse link is performed because there is no pilot signal for coherent detection. Thus, with the estimation of path delays via a sliding correlator, separable multipath components are assigned to each finger of the Rake receiver. Then, the equal-gain Rake receiver performs the demodulation in the following way. For each finger, the received I and Q signals are multiplied by the PNI and PNQ codes, so that the effect of code interference is separated. The value of I channel despread by the PNI code is denoted by $Z_{II}(m)$, where m denotes the mth symbol in 64-ary orthogonal modulation. Similarly, $Z_{IQ}(m)$, $Z_{QI}(m)$ and $Z_{QQ}(m)$ are obtained. Therefore, the decision variable for S_m can be written as[8]:

$$S_m = [Z_{II}(m) + Z_{QQ}(m)]^2 + [Z_{IQ}(m) - Z_{QI}(m)]^2 \qquad (5)$$

This noncoherent method can eliminate the phase distortion caused by the channel.

Ⅳ. Simulation results

The PCS simulator described above has been utilized and a single user has been assumed without loss of generality for our objective. The modulation scheme implemented in the simulator is QPSK rather than OQPSK for the purpose of reducing computation time. The number of branch (or finger) in the Rake receiver was limited to 3 in the simulation. It has been assumed that the time delay is perfectly estimated. A total of 80 power delay profiles were randomly generated and their values of the delay spread span from a fraction of microsecond up to approximately 18 microseconds. It should be noted that although some power delay profiles have the same (or similar) value of delay spread, the shape of those power delay profiles may quite differ. 80 profiles were applied to the simulator with the following simulation parameters. The carrier frequency was 1.8 GHz and the number of frames was 100. The mobile speed was 35 km, resulting in the maximum Doppler frequency of 58.33 Hz. The BER performance was obtained for a SNR of 3dB. For each profile, it is possible to obtain not only delay spread but also 7 more channel parameters described in Section 2.

Table 1. Correlation coefficient between wideband channel parameters and BER performance

SNR	Average delay	Delay spread	Delay interval at 5 dB	Delay interval at 10 dB	Delay interval at 15 dB	Delay window At 90%	Delay window at 75%	Delay window at 50%
3 dB	0.3482	0.0890	0.1298	0.0791	0.0822	0.0765	0.1362	0.2181

The correlation coefficient between the BER performance and each wideband channel parameter has been first examined. Table 1 shows the values of correlation coefficient obtained from the third order fitting curves. Among 8 possible scatter plots, the plots for the BER performance against delay spread and average delay are shown in Figure 3 and 4, respectively.

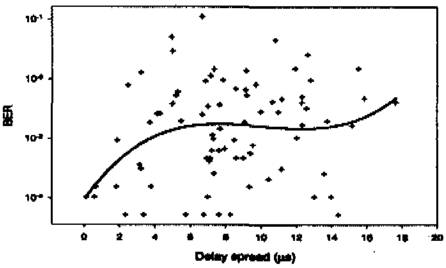

Figure 3. Delay spread vs BER performance

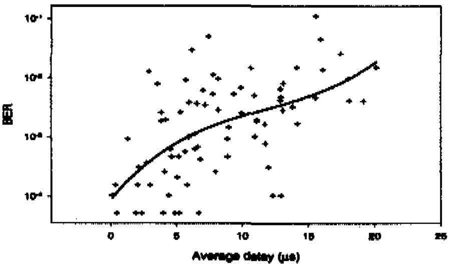

Figure 4. Average delay vs BER performance

Although the range of the performance variation is wide (i.e. relatively low correlation), it can be seen that the average delay has the best correlation with the performance. This observation is in direct contrast to the GSM system, where a relatively good correlation between the delay spread and the performance exists[1]. This finding can be illustrated below. The power delay profile shown in Figure 5 (PDP #61) has a delay spread of 1.812 s, whereas the power delay profile of Figure 6 (PDP #67) has a delay spread of 9.332 s. The actual BER performance is, however, identical with 0.000156 for a SNR of 3 dB. The reason for this is that although PDP #67 has

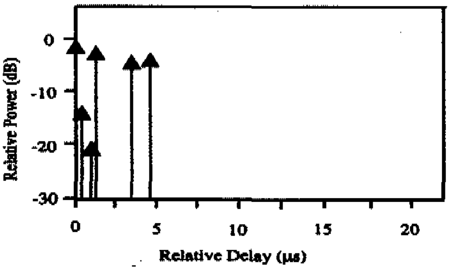

Figure 5. Power delay profile #61

large time dispersion, the first three paths are strong enough to provide sufficient path diversity via the Rake receiver. The performance is, therefore, not severely degraded.

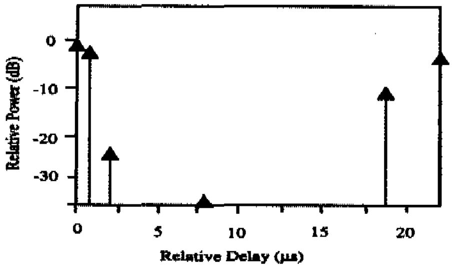

Figure 6. Power delay profile #67

The observation of the effect of delay spread on the performance has led to an investigation of the effect of power delay profile shape on the performance. For the present study, the following parameters were considered; the main profile (the first 3 echoes) length, the average attenuation of the main profile and the average attenuation of the second echo group. Figure 7 - 9 show the plots of the BER performance against the above profile parameters together with the third order fitting curves. Although the performance shows a wide variation over the profile parameters as expected, the following observation can be made.

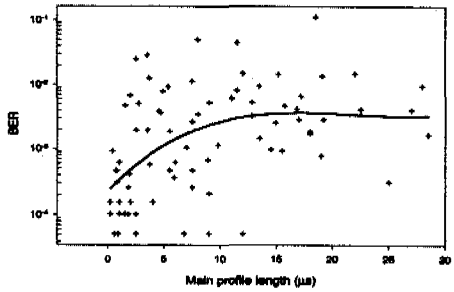

Figure 7. BER performance vs main profile length

From Figure 7, it can be seen that up to 10 s of the main PDP length, the performance degrades proportionally with increasing main profile length. For the values greater than that, the performance appears largely unaffected. Figure 8 shows that the performance begins to degrade when the relative power of the paths in the second echo group is larger than approximately -7 dB. The performance is also affected by the attenuation of the main profile. From Figure 9, we can clearly see that the performance is inversely proportional to the power level of the main profile. Therefore, it can be viewed that the power level of the main profile greatly influences the BER performance.

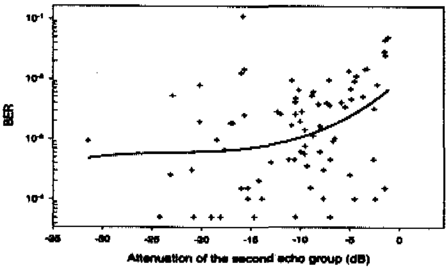

Figure 8. BER performance vs attenuation of the second echo group

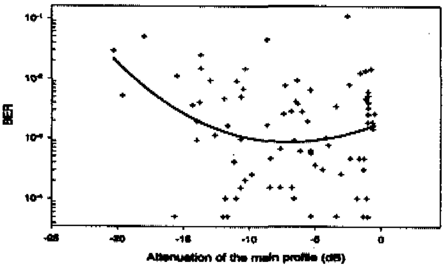

Figure 9. BER performance vs attenuation of the main profile

V. Conclusions

The effect of the time dispersion and power delay profile shape on the performance of a CDMA PCS system has been considered. The simulation results clearly indicate that, depending upon channel environments, the BER performance of a CDMA system has a wide variation. It has been found that unlike a TDMA-based system (e.g. GSM), delay spread does not show a good correlation with the performance in the CDMA PCS system. Instead, average delay has been found to have a better correlation. It can be thus concluded that as far as the CDMA PCS system is concerned, the delay spread is not as useful as in other wideband mobile radio systems, for relating to the BER performance. Taking the power delay profile shape into account, the performance has a wide variation, depending upon the power delay profile shape. This can be expected from the correlation values. Among the parameters of the PDP shape, the performance is more sensitive to the power level of the main profile (the first three paths).

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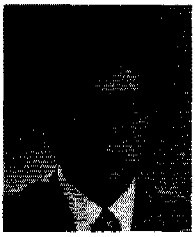

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