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ASIC Implementation of Pipelined OFDM-64QAM Wireless Indoor LAN Modem

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ABSTRACT

We present a ASIC(Application Specific Integrated Circuit) implementation of new high-speed pipelined wireless LAN modem for the ISM(Instrumentation, Scientific and Medical)-band indoor channel with low hardware complexity. 64QAM(Quadrature Amplitude Modulation) combined with OFDM(Orthogonal Frequency Division Multiplex) scheme is used for reliable higher data transmission rate of 6Mbps compared to a typical wireless LAN transmission rate of 2Mbps. A Pipelined and shared datapath architecture for IFFT/FFT and pilot-assisted channel equalizer are designed to improve the system performance at the reduced hardware complexity. The implemented ASIC chip uses 420,247 transistors and consumes power of 2.9W. The performance evaluation result shows 10-6 SER(Symbol Error Rate) at 29.3dB SNR(Signal to Noise Ratio), which satisfies the emission power regulation of IEEE 802.11.

I. Introduction

The advent of internet and multimedia communication requires mobility and easiness in transferring high-speed data at any place and time. Many drafts for wireless LAN standard are proposed to satisfy these requirements. IEEE 802.11 which specifies FHSS(Frequency Hopping Spread Spectrum), DSSS(Direct Sequence Spread Spectrum), and infrared methods does not satisfy these requirements[1]. The commercial products in compliance with the IEEE 802.11 have two disadvantages - low data transfer rate and high hardware cost. Transfer rate greater than 5Mbps is required for transmitting moving picture reliably. However, the maximum data transfer rate of the IEEE 802.11 limited to 2Mbps does not meet the QoS(Quality of Service) for multimedia communication. It is well known that the FHSS and DSSS methods use very wide frequency bandwidth for high-speed communication, and require dedicated complex circuit to resolve wide-band channel distortions[2][3][4]. Another method is using infrared technology requiring short coverage of LOS(Line of Sight) for reliable communication. The short coverage of LOS limits the mobility of the wireless modem. In order to solve the problems of the conventional wireless LAN modems, we develop a new OFDM-64QAM modem with reliable high performance. We use 64QAM which has frequency efficiency three times greater than that of QPSK[5][6]. OFDM is also used to avoid the problems associated with the frequency-selective fading[7][8](wide bandwidth channel), and to mitigate the effect of ISI(Inter-Symbol Interference). The OFDM combined with 64QAM offers high data transfer rate and robustness to channel distortions.

In section II, we briefly introduce the OFDM-64QA M system model. In section III, we introduce newly developed OFDM-64QAM modem simulator using SPW(Signal Processing Worksystem) for performance evaluation, and get

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논문번호 : 99381-0913, 접수일자 : 1999년 9월 13일
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modem parameters using the developed simulator. In section IV, the hardware architecture of transmitter is proposed, and the pipelined IFFT/FFT architecture with one shared butterfly operator is investigated intensively. In section V, we examine the architecture of the receiver with special attention on the architecture of channel distortion compensating circuit. In section VI, we describe the steps to implement ASIC chip and report on the power consumption, complexity, and performance as well. Finally, we draw a conclusion in section VII.

Ⅱ. System Model of OFDM-64QAM

In OFDM-64QAM system, data is transmitted simultaneously through parallel sub-channels occupying a small fraction of the signal bandwidth. The frequency responses of the sub-channels are orthogonal to each other for higher frequency efficiency[9]. The transmitted signal is given as

$$s(t) = \sum_{l=-\infty}^{\infty} x_{k,l}\,\phi_k(t-lT) \qquad (1)$$

$$\phi_k(t) = \begin{cases} \frac{1}{\sqrt{T}} e^{j2\pi\frac{W}{N}kt}, & \text{if } t\in[0,T] \\ 0, & \text{otherwise} \end{cases}$$

where, $\phi_k(t)$: sub-carrier
$x_{k,l}$: data symbol to be transmitted
T : The period of OFDM signal
N : The number of sub-carrier
W : The frequency bandwidth of transmitted signal

In Equation (1), frequency bandwidth of each sub-channels shrinks to W'(=W/N). OFDM-64QAM system has guard interval of T_{cp}. Guard interval is used to mitigate ISI due to the channel delay spread. OFDM-64QAM signal with duration of $T+T_{cp}$ is transmitted through a indoor radio propagation channel with its impulse response defined as[10]

$$g(t) = \sum_{l=0}^{\infty}\sum_{k=0}^{\infty} \beta_{kl}\, e^{j\theta_{kl}}\delta(t-T_l-\tau_{kl}) \qquad (2)$$

where, k : The number of ray
l : The number of cluster
β_l : Transmission gain
T_l : Cluster propagation delay
τ : Ray propagation delay with cluster
θ_{kl} : Phase shift
δ : Dirac delta function

The received signal via the channel can be written as

$$\begin{aligned} r(t) &= (g * s)(t) \\ &= \int_0^{T+T_{cp}} g(t)s(t-\tau)d\tau + n(t) \end{aligned} \qquad (3)$$

where, n(t) : Additive white Gaussian noise (AWGN)

Assuming that the sub-channels retain the orthogonality, matched filtering and sampling the received signal yields

$$\begin{aligned} y_k &= (r * \phi_k)(t)_{t=T} \\ &= \int_{-\infty}^{\infty} r(t)\phi(T-t)\,dt \\ &= \int_{-T}^{T_{cp}}\left(\int_0^{T_{cp}} g(\tau)\sum_{k=0}^{N-1} x_k\phi_k(t-\tau)\,d\tau\right)\phi_k^*(t)\,dt + n_k \\ &= \sum_{k=0}^{N-1} x_k h_k \int_{T_{cp}}^{T}\phi_k(t)\,\phi_k^*(t)\,dt + n_k \\ &= h_k x_k + n_k \end{aligned} \qquad (4)$$

where,

$$h_k = \int_0^{T_{cp}} g(\tau)e^{-j2\pi k\frac{W}{N}}d\tau$$

$$n_k = \int_{T_{cp}}^{T} n(T-t)\,\phi_k^*(t)\,dt$$

$$\int_{T_{cp}}^{T}\phi_{k'}(t)\,\phi_k^*(t)\,dt = \int_{T_{cp}}^{T}\frac{e^{j2\pi k'(t-T_{cp})W/N}}{\sqrt{(T-T_{cp})}}\frac{e^{-j2\pi k(t-T_{cp})W/N}}{\sqrt{(T-T_{cp})}}\,dt = \delta[k-k']$$

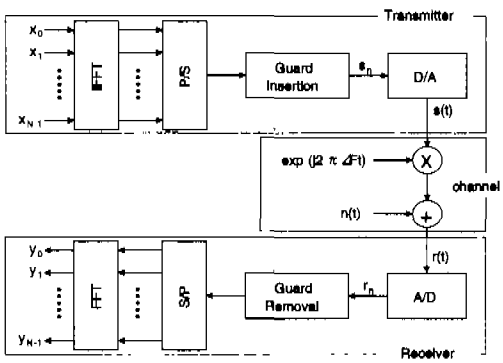

Fig. 1 System Model of OFDM-64QAM

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OFDM-64QAM system model defined by Equations (1), (2), (3), and (4) is shown in Figure 1. The sub-carriers are generated and are removed using the IFFT and the FFT respectively.

Ⅲ. OFDM-64QAM System Specification

We develop the OFDM-64QAM simulator using the SPW to evaluate the system performance and to determine the system parameters. Parameters such as the number of sub-carriers, the number of pilot signals, the pattern of pilot signal, and the duration of guard interval are critical factors that dominate the system performance. As the number of OFDM-64QAM sub-carriers gets larger, the frequency bandwidth of each sub-channel becomes narrower, and the system is more immune against frequency selective fading. Figure 2 shows the SER against various numbers of sub-carriers.

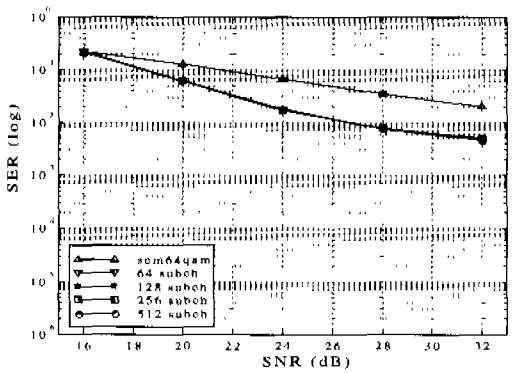
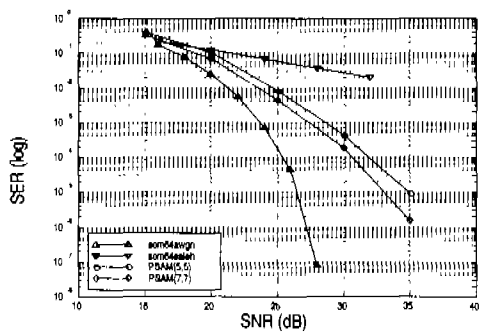


Fig. 2 Number of Sub-carriers vs. SER

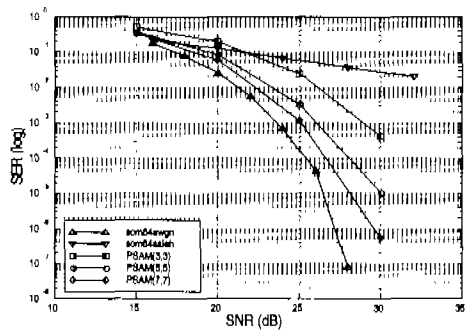
Since, SER performances with 128, 256, and 512 sub-carriers are similar in wireless indoor radio channel modeled by Saleh channel, we use 128 sub-carriers to reduce hardware complexity.

Pilot signal is used to estimate the wireless indoor radio channel distortions. Known data patterns are inserted on certain sub-channels at transmitter, and extracted at receiver to estimate the channel distortions. The number and pattern of pilot signals determine the performance of OFDM-64QAM system. As the number of pilot signals increases, the performance improves at the cost of increasing hardware complexity and transmission redundancy, as shown in Figure 3. The figure shows that the system performance is affected by the pilot pattern, and we choose equally spaced 8 pilot signals of (7d, 7d) constellation shown in Figure 4. The chosen pilot signals are inserted at 8, 24, 40, 56, 72, 88, 104, and 120 sub-carriers.

Guard interval is a cyclic prefix of OFDM-64QAM signal to mitigate ISI. If we set the guard interval longer than the maximum channel delay spread, the effect of ISI is minimized. Guard interval is also used for frame synchronization and carrier recovery because the guard interval is made of a cyclic prefix of OFDM signal. By correlating guard interval with the rest of OFDM signal, we get frame synchronization when maximum correlation is detected. Selected guard interval is 10μs. The system parameters are obtained by simulation, and are summarized in Table 1.



(a) No. of Pilot Signal = 4



(b) No. of Pilot Signal = 8

scm64awgn : Single Carrier 64QAM modulation in AWGN channel

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scm64saleh : Single Carrier 64QAM modulation in Saleh Channel
PSAM(3,3) : Pilot Assisted OFDM-64QAM modulation in Saleh channel with (3d, 3d) pilot pattern
PSAM(5,5) : Pilot Assisted OFDM-64QAM modulation in Saleh channel with (5d, 5d) pilot pattern
PSAM(7,7) : Pilot Assisted OFDM-64QAM modulation in Saleh channel with (7d, 7d) pilot pattern

Fig. 3 Number and Pattern of Pilot Signal vs. SER

Table 1. OFDM-64QAM System Parameters

Modulation Scheme	64QAM
Transmission Method	OFDM
No. of Sub-carriers	128
Guard Interval	10us cyclic prefix of OFDM-64QAM signal
Pilot Signal	equally spaced 8 pilot signals (7d, 7d)
Sub-carrier Generation	128 point IFFT/FFT
Channel Equalization	1-tap LMS equalizer
Synchronization Method	frame/carrier/clock synchronization using MLE(Maximum Likelihood Estimation)
System Clock	48MHz
Transmission Rate	6Mbps
Signal Duration	138μs

Ⅳ. Transmitter Architecture

As shown in Figure 5, transmitter consists of serial-to-parallel buffer, 64QAM mapper and pilot signal insertion block, IFFT/FFT block, and guard interval insertion block.

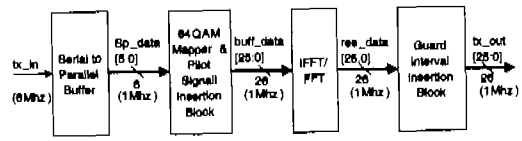

Fig. 5 The architecture of transmitter

The serial-to-parallel buffer converts the 1-bit serial signal into 6-bit signal. The 64QAM mapper converts the parallel signal into 64QAM modulated 26-bit complex block floating point signal. IFFT/FFT transforms it into 26-bit OFDM signal.

We design radix-2 DIF(Decimation in Frequency) IFFT/FFT for removal and generation of OFDM sub-carriers with minimal hardware complexity. The datapath circuit within IFFT/FFT block perform addition and multiplication of two 26-bit block floating point numbers to minimize error from rounding and overflow. In order to complete transformation, series of seven stage butterfly computations are required. The calculation results in rounding error leading severe inaccuracy as shown in Table 2.

Table 2. Relationship between Bit Length and Error Rate

Bit Length	Error Rate (Error/Signal)	Circuit Size (Multiplier)	Circuit Size (Adder)
10	48%	A	B
13	1.07%	1.25A	1.59B
16	0.202%	1.52A	2.35B

The table shows that the error rate can be reduced dramatically if bit length of 26 is used instead of 20. This reduction trades off the size of two datapath circuits composing the butterfly operator. Considering hardware complexity and

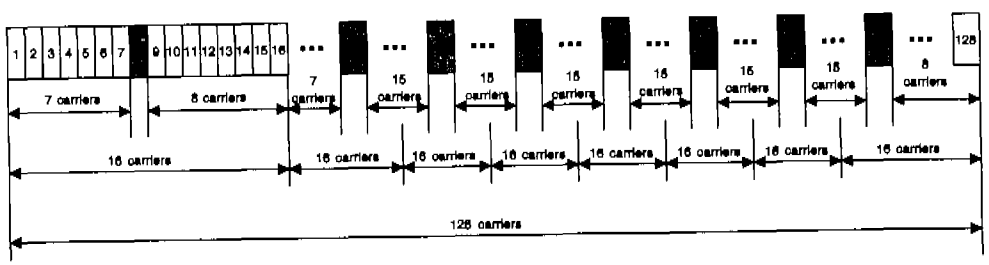

Fig. 4 Configuration of Pilot Signal

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accuracy, we use 26-bit complex block floating point number system as shown in Figure 6. Typical IFFT/FFT circuit employs multiple butterfly operators, which increase hardware complexity[11]. For our implementation, we use a single pipelined radix-2 butterfly operator to minimize the hardware complexity while maintaining high throughput. Designed 7-stage pipeline is shown in Figure 7.

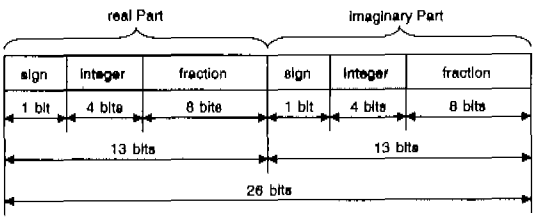

Fig 6 26-bit Block Floating Point Number Format

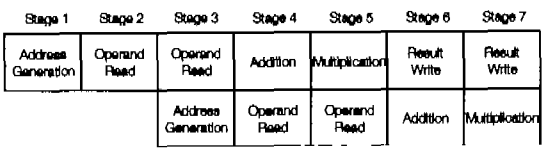

Fig. 7 Pipeline Stage of Butterfly Operator

Designed pipeline is optimized to perform 128 point Fourier transformation of the input signal within one OFDM signal duration(=138us), and several registers with multiplexers are used for the pipeline control. As shown at figure 7., the designed IFFT/FFT does butterfly operations at every second clock and requires only 896 clocks for 128 point IFFT/FFT. The IFFT/FFT block performs real-time transformation using three memories. Buffering the input signal, storing the results of butterfly operations, and fetching the results of fourier transformation are carried out simultaneously using these memories. Two typical and one special addressing mode are supported. Normal and bit-reversal addressing mode are used in conventional FFT processors. A new addressing mode, called reverse order addressing mode, is used for doing guard interval insertion with minimal circuit size. The guard interval is a cyclic prefix copied from the last part of IFFT results. Inserting guard interval without reverse order addressing mode requires 128-word* 26-bit memory to hold IFFT results until the last result is fetched. Using the reverse order addressing mode, the guard interval is inserted without using memory as shown in Figure 8.

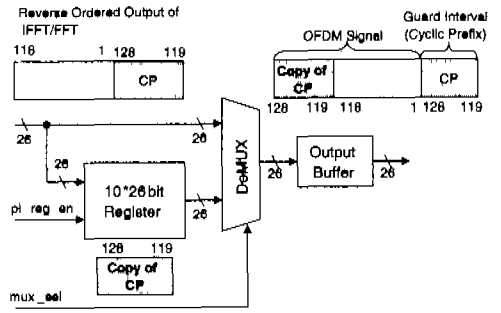

Fig. 8 Guard Interval Insertion Using Reverse Order Address Mode

The architecture for the implemented IFFT/FFT block is shown in Figure 9.

V. Receiver Architecture

Receiver consists of guard remover, IFFT/FFT block, pilot-assisted channel distortion compensating block, frequency domain equalizer, pilot extractor, 64QAM demapper, parallel-to-serial converter, and synchronization block.

The distorted guard interval of received signal is removed at guard remover, and the result signal is transferred to IFFT/FFT block for removing 128 sub-carriers. Pilot-assisted channel distortion compensating block and frequency domain equalizer compensate for multi-path distortions. Finally, transmitted signal is recovered after 64QAM demapping. On the receiver, frame synchronization and carrier recovery are also done by performing cyclic convolution between guard interval and the OFDM signal. The architecture of receiver is shown in Figure 10.

1. Pilot-assisted Channel Distortion Compensating Block

Pilot-assisted channel distortion compensating block compensates for the channel distortion by Equation 5.

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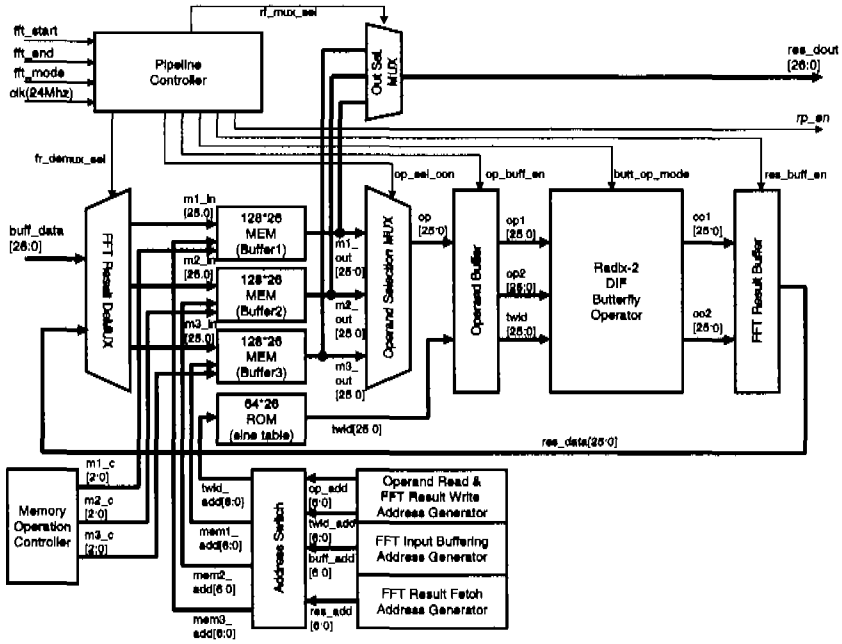

Fig. 9 Architecture of IFFT/FFT Block

$$PC(t) = RS(t) \times \frac{\{P(t) \times PS^*\}^*}{|P(t)|} \qquad (5)$$

where, PC : Compensated data signal

RS : Received data signal

P : Received Pilot signal

PS : Transmitted pilot signal

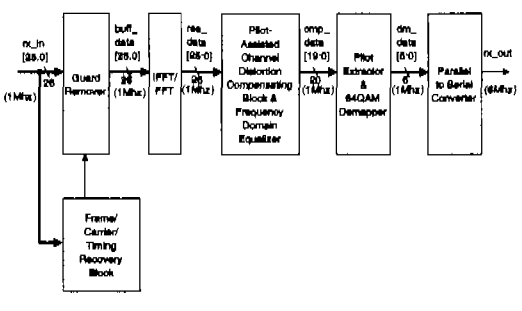

Fig. 10 Receiver Architecture

This block performs compensating operation by estimating normalized phase offset, and then subtracting the offset from received signal. The block requires two complex multiplications, one square root calculation, and one division as shown Table 3.

Table 3. Pilot Assisted Channel Compensation Operation

Operation	Sub-operation	Op. A	Op. B	Result Storage
① calculate offset of pilot	$P_r \cdot PS_r^*$	P_r	PS_r^*	mul1
	$P_i \cdot PS_i^*$	P_i	PS_i^*	mul2
	$P_r \cdot PS_r^* - P_i \cdot PS_i^*$	mul1	mul2	mul_r
	$P_r \cdot PS_i^*$	P_r	PS_i^*	mul1
	$P_i \cdot PS_r^*$	P_i	PS_r^*	mul2
	$P_r \cdot PS_i^* + P_i \cdot PS_r^*$	mul1	mul2	mul_i
② calculate square of offset	$mul_r \cdot mul_r$	mul_r	mul_r	mul1
	$mul_i \cdot mul_i$	mul_i	mul_i	mul2
	$mul_r \cdot mul_r + mul_i \cdot mul_i$	mul1	mul2	off_mag
③ calculate square root of offset	Sqrt(off_mag)	off_mag		PM
④ calculate normalized offset	PO_r/PM_r	mul_r	off_mag	$noff_r$
	PO_i/PM_i	mul_i	off_mag	$noff_i$
⑤ calculate compensated symbol	$RS_r \cdot noff_r$	RS_r	$noff_r$	mul1
	$RS_i \cdot noff_i$	RS_i	$noff_i$	mul2
	$RS_r \cdot noff_r - SYM_i \cdot noff_i$	mul1	mul2	PC_r
	$RS_r \cdot noff_i$	RS_r	$noff_i$	mul1
	$RS_i \cdot noff_r$	RS_i	$noff_r$	mul2
	$RS_r \cdot noff_i + RS_i \cdot noff_r$	mul1	mul2	PC_i

According to Table 3, these sequential operations can be performed by sharing one adder, one multiplier, one square root calculator, and one divider reducing hardware complexity.

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Demultiplexer with symbol delay buffer for pilot signal extraction and three multiplexers with thirteen registers for datapath sharing control are used to design shared architecture as shown in Figure 11. The integer extension circuit is used for extending 26-bit complex block floating point number into 34-bit complex block floating point to prevent overflow during calculation of the square value of RS. This shared architecture reduces the number of used transistors from 140,993 to 60,829.

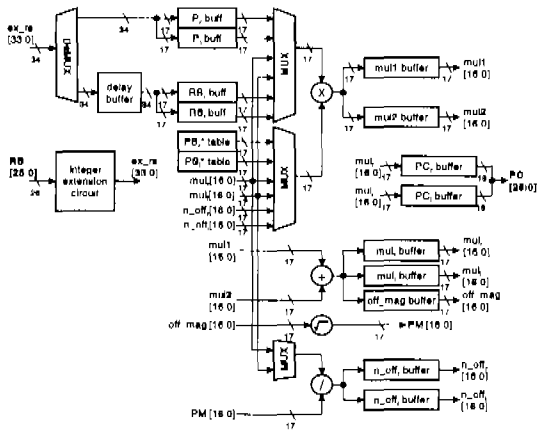

Fig. 11 The Architecture of Pilot-assisted Channel Distortion Compensating Block

2. Frequency Domain Equalizer

In OFDM-64QAM system, a simple equalizer is adequate for channel equalization because each sub-channel's bandwidth is 7.812KHz and ISI is removed by guard interval. 1-tap LMS(Least Mean Square) equalizer is good enough to equalize the received signal. Although frequency domain equalization requires 128 equalizers for each sub-carrier, we only use one shared 1-tap LMS equalizer and two 128-word*26-bit memory. The 1-tap LMS equalization is described in Equation 6.

$$ES_n(t) = RS_n(t) + \{[d_{n-1}(t) - ES_{n-1}(t)] \times STF + WN_{n-1}\} \times RS_n^*(t) \quad (6)$$

where, ES_n : Equalized data signal

RS_n : received data signal

d_{n-1} : 64QAM demapped value of ES_{n-1}

STF : Step value

WN_n : Weight factor

$\{[d_{n-1}(t) - ES_{n-1}(t)] \times STP + WN_{n-1}\} \times RS_n^*(t)$

ER_n : Error factor

$(d_{n-1}(t) - ES_{n-1}(t)) \times STF$

The equalization described above requires two complex multiplications and three complex additions as shown Table 4. However these sequential operations can be done by sharing one adder and one multiplier with minimal hardware complexity. The proposed equalizer operates with one adder and one multiplier at 16Mhz clock by employing our shared architecture. Sixteen registers and four multiplexers are used to control pipeline operation, and two 128-word*26-bit memories with address generator are used to store error and weight factor of each sub-carriers. The architecture is shown in Figure 12. This shared architecture reduces the number of used transistors from 88,829 to 53,349.

Table 4. 1-tap LMS Equalization Operation

Operation	Sub-operation	Op. A	Op. B	Result Storage
① calculate complex conjugate of X	none	X		X*
② calculate ER • X*	$ER_r \cdot X_r^*$	ER_r	X_r^*	$mul1$
	$ER_i \cdot X_i^*$	ER_i	X_i^*	$mul2$
	$mul1 + mul2$	$mul1$	$mul2$	mul_r
	$ER_r \cdot X_i^*$	ER_r	X_i^*	$mul1$
	$ER_i \cdot X_r^*$	ER_i	X_r^*	$mul2$
	$mul1 + mul2$	$mul1$	$mul2$	mul_i
③ calculate ER • X* + WN	$WN_r + mul_r$	WN_r	mul_r	add_r
	$Wn_i + mul_i$	WN_i	mul_i	add_i
④ calculate X + (ER • X* + WN)	$mul1 + mul2$	X_r	add_r	ES_r
	$mul1 + mul2$	X_i	add_i	ES_r
⑤ decode	none	mul_r	mul_i	d
⑥ calculate d - [X+(ER • X* + WN)]	$d_r - mul_r$	d_r	mul_r	add_r
	$d_i - mul_i$	d_i	mul_i	add_i
⑦ calculate ST • {d - [X+(ER • X* + WN)]	ST • add_r	ST	add_r	mul_r
	ST • add_r	ST	add_i	mul_i

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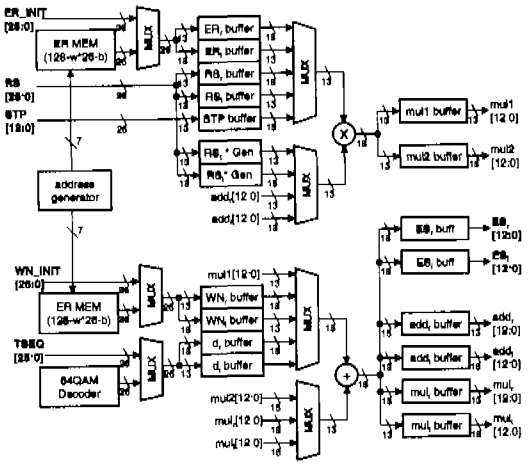
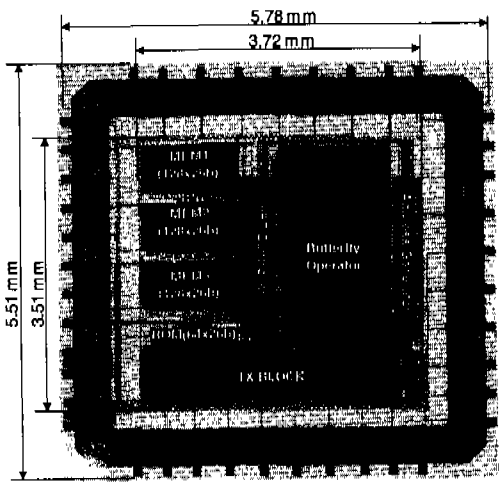


Fig. 12 The Architecture of Equalizer

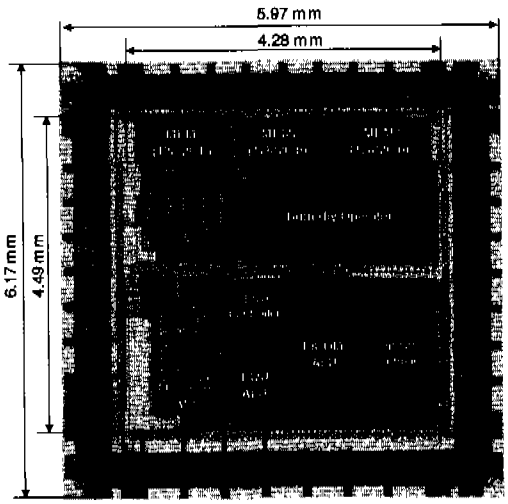
Ⅵ. ASIC Implementation

We implement the OFDM-64QAM modem using 0.6μm 1-poly, 3-metal process The hardware design is based on algorithm verification using the SPW simulator.

The proposed architecture is coded in HDL and is synthesized by ASIC synthesizer. The timing, area, and power estimation of the synthesized design are also performed. The physical implementation is carried out by commercial placement and routing tools as shown in Figure 13.



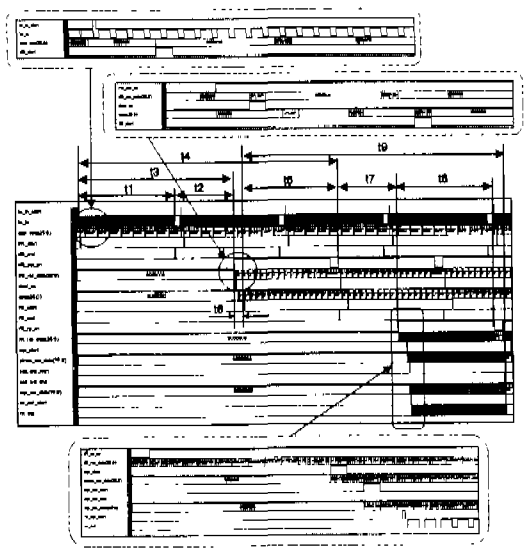
(a) Transmitter



(b) Receiver

Fig. 13 Layout of Transmitter and Receiver

According to the result of post-layout simulation shown in Figure 14, the implemented modem requires 347.73μs and 352.07μs for modulation and demodulation process respectively.



* t1 : IFFT operand buffering time(=128μs)
t2 : IFFT operation time(=81.73μs)
t3 : First IFFT result fetching time(=209.73μs)
t4 : Modulation time(=347.73μs)
t5 : FFT operand buffering time(=128μs)
t6 : Guard interval(=10μs)
t7 : FFT operation time(=81.73μs)
t8 : FFT result fetching time(=128μs)
t9 : Demodulation time(=352.07μs)

Fig. 14 Post-layout Simulation

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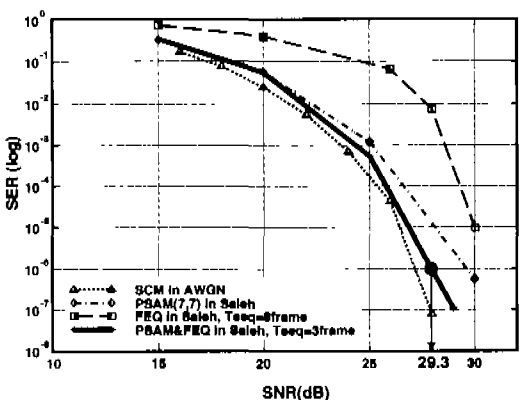
The operation of IFFT/FFT requires only 81.72 ㎲. The power consumption is estimated using gate-level power estimation tool. Capacitance and resistance are back-annotated from layout. The estimated power consumption is to be 0.936W and 1.963W for transmitter and receiver respectively at 3.3 volt for random test vector. The number of transistors used for the implemented modem is shown in Table 5. The performance estimation shows 10^{-6} SER(Symbol Error Rate) at 29.3dB SNR(Signal to Noise Ratio) as shown in Figure 15.

Table 5. Transistor count of transmitter and receiver

Transmitter		Receiver	
IFFT/FFT	135,340	IFFT/FFT	135,340
		Pilot-assisted Channel Distortion Compensater	60,829
others	30,674	Frequency Domain Equalizer	53,349
		others	4,715
Total	166,014	Total	254,233



* SCM in AWGN : Single carrier 64QAM modulation in AWGN channel

PSAM(7,7) in Saleh : Pilot signal assisted OFDM-64QAM in Saleh channel

FEQ in Saleh, Tseq=8frame : OFDM-64QAM with frequency domain equalizer in Saleh channel using 8 frame training sequence

PSAM & FEQ in Saleh, Tseq=3frame : Pilot signal assisted OFDM-64QAM with frequency domain equalizer in Saleh channel using 8 frame training sequence(proposed modem)

Fig. 15 SER of OFDM-64QAM Modem

Ⅶ. Conclusion

We developed a new high-speed wireless indoor LAN modem chip set. Transmission scheme employs OFDM combined with 64QAM for reliable high speed data transmission of 6Mbps in 2.4GHz ISM-band. We have designed the modem in pipelined and shared architecture for consistent throughput at 48MHz system clock with low hardware complexity. The total number of used transistors is 420,247. The dimension of the transmitter ASIC implemented using 0.6㎛ 1-poly, 3-metal process is 3.72×3.51㎟ without pads and 5.78×5.51㎟ including pads, and the dimension of receiver ASIC is 4.28×4.49㎟ without pads and 5.97×6.17㎟ including pads. The power consumption of 2.9W is suitable for portable application, and the estimated SER of 10^{-6} at 29.3 dB SNR satisfies the emission power regulation of IEEE 802.11. The possible application of the designed modem includes wireless POS(Point of Sale) system, wireless multimedia terminal, DVB(Digital Video Broadcasting) and DAB(Digital Audio Broad- casting) systems.

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