IMT-2000 시스템을 위한 광대역 CDMA 채널 카드 및 복조기의 설계 및 구현

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Design and Implementation of Wideband CDMA Channel Card and Demodulator for IMT-2000 System

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요 약

본 논문은 CDMA 2000 Radio Transmission technology (RTT) 규격에 기초한 International Mobile Telecommunication - 2000 (IMT-2000) 시스템을 위한 광대역 CDMA 기지국 채널 카드 및 복조기의 설계, 구현 및 시험에 관해서 서술했다. 구현된 기지국 복조기의 성능을 측정하여 얻은 결과를 이론적인 성능과 비교 하였다. 또한 구현된 복조기가 실장 된 시스템은 음성 (9.6Kbps), 실시간 동영상 (384Kbps) 및 데이터 서비스 (144Kbps)에 기초한 인터넷 프로토콜 등과 같은 무선 서비스를 제공해 준다.

ABSTRACT

This paper describes the design, implementation and testing of wideband code division multiple access (CDMA) base station demodulator for the international mobile telecommunication-2000 (IMT-2000) system test plant based on cdma2000 radio transmission technology (RTT). The performance of the implemented base station demodulator is measured and compared with the theoretical performance bound. The system test plant equipped with this demodulator provides wireless services, such as high quality speech (9.6kbps), real-time video (384kbps) and internet protocol (IP) based data services (144kbps) in a mobile radio environment.Z

Ⅰ. 서 론

Most of wireless communication systems currently being used, such as the second generation digital cellular and personal communication service (PCS), are primarily focused on relatively low rate voice-oriented services. In case of IS-95 based CDMA system, which is also called as narrow band CDMA system, the relatively low chip rate (1.2288 Mcps) has been regarded as high enough. These days the demand for other types of services, such as wireless packet data and wireless multimedia, are growing rapidly. But it has been found that current systems do not satisfy the emerging demands higher data rates and at the same time enhanced quality of service. To overcome the shortcoming of the second generation CDMA systems and extend their capability, a new generation mobile radio service, namely IMT-2000, is proposed and its standardization process is in its final stage under ITU-R. After evaluating several RTTs proposed, IMT-

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논문번호 : 00269-0714, 접수일자 : 2000년 7월 14일

2000 RTT standard will be selected. Among them, RTTs based on Wideband direct-sequence spread-spectrum (DS-SS) CDMA technique [1],[2] are considered as key candidates for satisfying the requirements of the third generation mobile radio systems.

Electronics and Telecommunications Research Institute (ETRI) in Korea has developed IMT-2000 System Test Plant (STP) to evaluate ETRI's RTT [3], and to develop wideband CDMA modem technologies, application services, and wireless ATM network systems. ETRI's RTT is based on wideband CDMA technology and is somewhat similar to that of cdma2000. But it is not the same as RTTs proposed by Korea; namely Telecommunication Technology Association (TTA) proposal I [4] and TTA proposal II [5]. The key parameters of RTT used in STP are chip rates of 3.6864Mcps, RF bandwidths of 5MHz, and data rate of up to 384 kbps.

For the implementation of the demodulator in digital communication system, quantization process is necessary and the number of bit assignment to received symbols is a critical factor. In this paper, integer simulation is done for the efficient implementation of demodulator in reverse link, and these simulation results are used for the implementation of the demodulator. The power ratio of pilot channel to traffic channel, and integration length of phase estimation, quantization process are analyzed and each optimal parameters are obtained. Using these parameters, the demodulator in reverse link is implemented and system equipped with this demodulator provides wireless services such as high quality speech, real-time video and internet protocol based data services.

In this paper, we focus on the design concept and the implementation of base station demodulator and channel card of STP. In section II, we introduce ETRI's IMT-2000 RTT and overall structure of the STP system. Design concept and implementation issues of STP base station demodulator are described in Section III. The performance of the implemented demodulator is discussed in Section IV, followed by summary and conclusions in Section V.

Ⅱ. RADIO TRANSMISSION TECHNOLOGY AND SYSTEM TEST PLANT

1. RADIO TRANSMISSION TECHNOLOGY

Table 1 briefly describes the key characteristics of RTT used in the developed IMT-2000 STP. RTT is based on the wideband DS-SS CDMA technology. Forward link and reverse link are separated by frequency division duplex (FDD) method, and their carrier frequencies are 2110.05~2169.95 MHz and 1920.05~1979.95 MHz, respectively. The frame length is 20 ms, and the period of the short PN codes is 26.667ms. RTT uses chip rate of 3.6864 Mcps, which requires about 5MHz bandwidth. Convolutional channel coding is used for voice data service and turbo coding for image and packet data services. There are pilot, sync, paging, traffic (fundamental or supplemental), and dedicated control channel in the forward link. The reverse link consists of pilot, traffic (fundamental or supplemental), access and dedicated control channel.

The fundamental traffic channel is used for voice data service and supplementary channel is used mainly for packet data services for internet access, video, slow-scan video, and picture transfer services. The control data messages are transmitted via dedicated control channel. The quadrature phase shift keying (QPSK) data modulation is applied and the pilot channel is I/Q multiplexed before QPSK spreading. The orthogonality between the reverse link channels is maintained by the Walsh codes, and the reverse link channels for each mobile stations are distinguished by long codes with different time offsets. Antenna diversity is used for better performance in the base station.

For transmit power control operation, signal-to-interference ratio (SIR) is measured at the rake receiver and is compared with the target SIR. The rake receiver generates the transmit power control

command which is transmitted to the mobile via the forward link to raise or lower the transmit power. The pilot channel is time multiplexed with power control bits. In the reverse link, continuous pilot scheme is used for coherent detection.

Table 1. The RTT for the implemented IMT-2000 STP

Multiple Access	Wideband DS-CDMA
Duplex	FDD
PN Chip Rate	3.6864 Mcps
Frame Size	20 ms
Channel bandwidth	5MHz
Channel Coding	Convolutional/Turbo Coding
Channel Structure	FL:Pilot/Sync/Paging/Traffic/Signaling RL:Pilot/Access/Traffic/Signaling
Spreading Codes	Short PN code, Long PN code
Signaling Channel	Dedicated code channel for signaling
Orthogonal Codes	Walsh code
Diversity	Rake and Antenna
Power Control	SIR-based TPC
Inter-cell Synchronization	Synchronous
Data modulation/ PN Spreading	FL/RL:QPSK/QPSK
Coherent Detection	RL:Pilot time multiplexed with PC

(FL : Forward Link , RL : Reverse Link)

2. RADIO TRANSMISSION TECHNOLOGY

Figure 1 shows the overall system architecture of the developed IMT-2000 STP. The STP consists of mobile stations (MSs), base stations (BSs), base station controllers (BSCs), location register /authentication center (LR/AC), inter-working functions (IWFs), and mobile switching center (MSC). The BS consists of RF transceiver unit, IF conversion and clock generation unit, packet switching unit, channel card and base station control processor (BCP). The RF unit converts the received RF signal to IF signal, which is a down-converting to the baseband. The baseband signal is converted to digital signal and demodulated at the channel card(CC). PN despreading, demodulating, rake combining and channel decoding operations are performed at the CC block. For the forward link, channel card encodes and modulates the information signal, then the signal is up-converted to the IF band. It is then sent to RF unit for up-conversion to RF band and transmitted to the mobile station. Each channel card has two modulation and demodulation modules each of which can be operated as control or traffic (fundamental or supplementary) channels. Demodulator is designed to support two orthogonal code channels that can be configured to support data rates of 9.6 kbps and 144kbps or 384 kbps, independently. The packet switching unit is a packet router between BS and BSC. Control and Data information is passed to the destination by this switching unit. BCP controls call processing and device initialization. It is responsible for the management of resources in the base station.

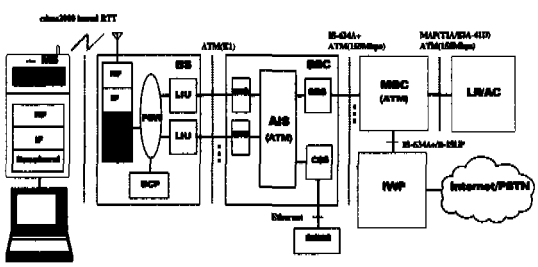


Fig. 1 The overall system architecture of the IMT-2000 STP

Ⅲ. MAJOR BLOCK IMPLEMENTATION OF DEMODULATOR

Figure 2 shows the base station channel card that includes controller module, demodulation module and peripheral devices for communication with other elements in BS. To simplify implementation and increase flexibility, TMS320C6201 digital signal processor (DSP) and field programmable gate array (FPGA) are used; DSP is used for implementation signal processing algorithms and FPGA is used for the control logic. Demodulation module consists of code acquisition module (or searcher) for initial (or coarse) synchronization and code tracking & data demodulation module for fine synchronization and data demodulation.

For mobile communication systems using spread spectrum technology, the exact phase estimation of incoming pseudo-random (PN) sequence is very important. PN code synchronization is usually accomplished in two steps: code acquisition and code tracking. Code acquisition is the initial search process that brings the phase of the locally generated code to within a chip duration of the incoming code. Code tracking is the process of achieving and maintaining fine alignment of chips boundaries of the incoming and locally generated PN codes.

For detail implementation of description on code acquisition, code tracking and demodulation module, see references [6],[7].

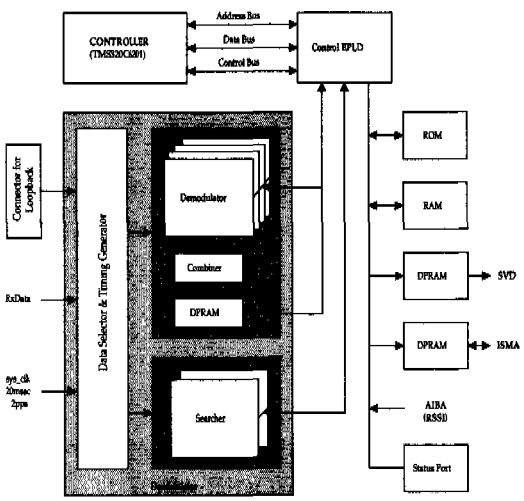


Fig. 2 Block diagram of the channel card (CC) in the base station

1. PN CODE ACQUISITION

As shown in figure 3, the code acquisition module is composed of data mapping block, long and short PN code generator, 16 correlation blocks, sorting and control block. The received RF band signal is first down converted to base band frequency and then its data components are digitized with asynchronous 4-bit analog to digital converter operating at a system clock of 29.4912 MHz. The resulting samples, which are over sampled eight times of the PN chip rate, are passed through Data Mapping block. Data Mapping block selects one of among six signals from two antennas and three sectors. Then, it performs data format conversion and scaling. The resulting sampled data has 2' s complement format with range of -15~15. This is the input data of correlator. The PN generator block supplies a PN code and delayed PN code to the correlation block. Serial search scheme is applied to the code acquisition module for simple hardware structure. Code acquisition module is for the initial search process that brings the phase of the locally generated PN code to within 1/2 chip duration of the incoming data. We find a PN offset that has maximum correlation value in the range of a search window size. The four PN offset values and searching energies are stored in the Sorting block according to the order of the searching energies. These values are sent to the controller and are used to update the code tracking mode.

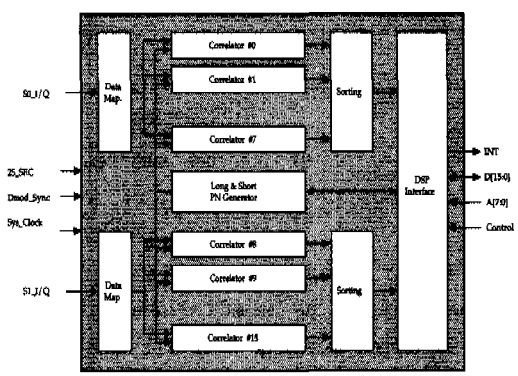


Fig. 3 Block diagram of code acquisition module

2. CODE TRACKING AND DATA DEMODULATION

Using the PN offset acquired in the code acquisition module, code tracking module finds and keeps fine alignment of chip boundaries of incoming code to that of locally generated PN code. The functional block diagram of code tracking and data demodulation module is shown in figure 4.

Code tracking and data demodulation module includes data decimator and PN code generator, demodulation block, code tracking block, symbol combiner, lock detector and DSP interface block.

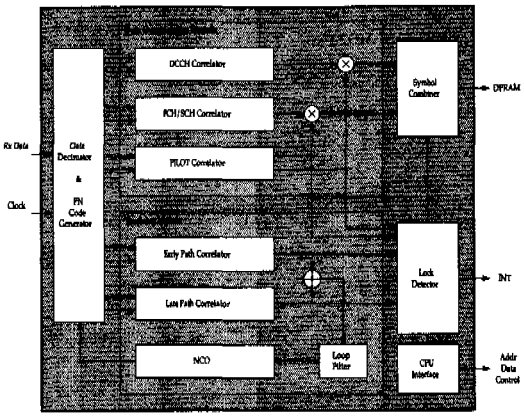


Fig. 4 Block diagram of code tracking and data demodulation module

Data demodulation block consists of four fingers that can demodulate 4 separate paths signals.

The operation of the code tracking module is as follows: If BS was synchronized to MS in figure 1, the early/late correlator would have a correlation value. But if there was a timing error between BS and MS, early correlator and late correlator will be of different values. Using the difference between these two correlator values, code tracking loop controls the phase of local PN code, and tracks and keeps the synchronization between the transmitter PN code and the receiver PN code. Code tracking module consists of decimator, early correlator, late correlator, loop filter and numerical controlled oscillator (NCO). Decimator selects a signal among input signals oversampled-by-8. Data sample for data demodulation is also selected at the decimator. To reduce the complexity of code tracking loop, the input data to early/late correlator and data demodulator are set to be separated by Tc/2. Early and late correlator measures the phase correlation between local PN code and the data sample selected by the decimator. Comparing the sign bit of the data sample with the phase of local PN code, they add data sample to accumulator or subtract it from accumulator for the integration length duration. After correlation, the energy is calculated by summing the squared correlation values of I and Q data. The difference between energies of early and late path is fed into the loop filter and the energy is averaged over integration length. The output of the loop filter is used in controlling NCO (numerically controlled oscillator), which generates clock frequency of the clock according to the input number. It works as a VCO in analog PLL. PN code generator and decimator use the output of NCO as a clock, and adjust the phase of local PN code to that of the received signal. Figure 5 shows the timing diagram of the early-late correlator.

Once the mobile and the base station are synchronized through successful tracking, i.e., phase locked, the demodulator will get correct I and Q data. The system estimates phase delay using pilot signal for coherent demodulation, assuming that it does not change during estimation. The received signal is multiplied by pilot Walsh code and PN code, and then is integrated during estimation period. To eliminate cross-talk between I and Q channels, integrated digital samples for I and Q channels are added to or subtracted from each other. The resulting I and Q channel samples are normalized and represents the phase delay estimate. Data is demodulated using similar steps as the phase delay estimation. Digital samples of the received signal are multiplied by I and Q channel Walsh code of traffic channel, PN code, and I and Q channel phase estimates, and are integrated for one symbol period. Cross-talk are eliminated by adding or subtracting digital samples of I and Q channels, as is done in the phase estimation.

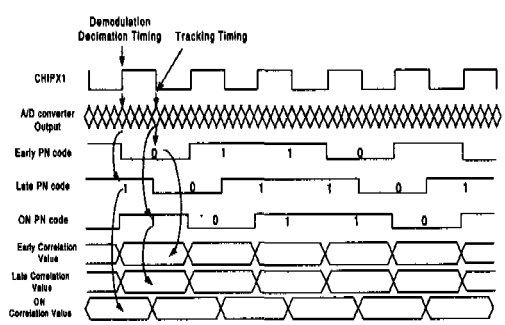


Fig. 5 Timing diagram of early-late correlator

3. COMBINER AND DEINTERLEAVER

As the multipath signals from the fading channel have suffered from different time delays, the demodulated symbol of each finger is not synchronized to those of other fingers. Therefore, the compensation of the different time delay of each path is necessary before combining them. Deskewing buffer is used for this purpose. Round trip delay (RTD) of each path is calculated, and deskewing buffer reads the demodulated symbol stored at FIFO considering this RTD. The data stored in the deskewing buffer is all aligned. The time-aligned multipath signals are combined at combiner. Figure 6 shows the timing diagram of the Combiner.

The combined symbols are sent to DSP by way of DPRAM for deinterleaving. Compared to the deinterleaver of IS-95, IMT-2000 RTT is much bigger and more complicated, thus high speed operation is essential in reducing the processing delay. It is implemented by DSP, which has both flexible implementation of deinterleaving algorithms and debugging. To optimize its processing speed, assembly language is used in the core module of deinterleaving software. The deinterleaved symbols are sent to Viterbi decoder at demodulator board by way of DPRAM. To lessen the processing load of the DSP, it only writes deinterleaved symbols to DPRAM. Then, control FPGA read, the data from DPRAM and sends them to Viterbi decoder.

4. POWER CONTROL

CDMA is known as interference-limited system in the sense that the system capacity is closely related to the amount of interference. The maximum capacity is achieved when the power control is performed perfectly. For the effective power control, the implemented system employs two kinds of power control schemes; open-loop power control and fast closed-loop power control. Closed-loop power control includes reverse link and forward link power control operations, which is related to the BS demodulator.

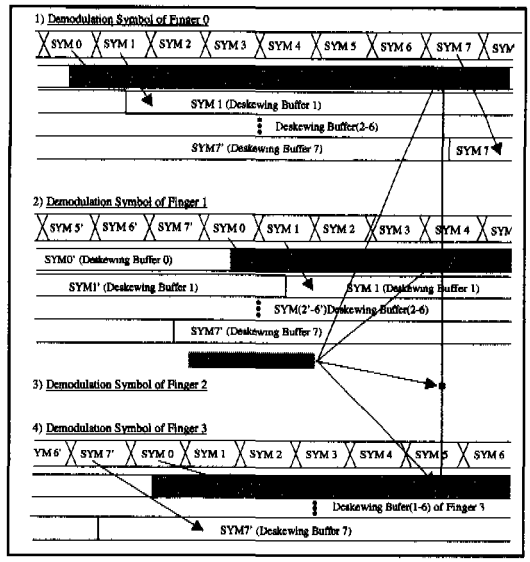


Fig. 6 Timing diagram of combiner

The reverse link power control scheme is performed by the power control command from the BS demodulator. The BS demodulator receives the threshold value (Eb/N0)set point from the base station controller (BSC) every 20 ms. Also, it measures the strength of the received signal and estimates Eb/N0 based on the measurements at every power control group (1.25 ms). If the measured Eb/N0 is greater than the desired one (Eb/N0)set_point, BS sends a command to MS to adjust the transmit power downwards. Power control commands are sent to MS through the power control sub-channel. The power control bit is not coded. The command bit punctures the coded symbols in the randomized position. This power control bit puncturing is performed in the BS modulator. The forward link power control is performed by the power control command from the MS demodulator. The forward link power control scheme is similar to the reverse link power control.

Ⅳ. EXPERIMENTAL RESULT

Based on computer simulation, we implemented the BS demodulator as shown in figure 7. To evaluate the performance of the implemented BS demodulator, PN code rate of 3.6864 Mcps and

carrier frequency of 2 GHz were used. It is assumed that the transmitted signal undergoes an additive white gaussian noise (AWGN) channel. Data rates for traffic and control channel are set to be 9.6 kbps. Transmit power of pilot channel is 6 dB less than that of traffic or control channel. Figure 8 shows the QPSK constellations of the implemented BS demodulator. Figure 9 shows the detection probability of the code acquisition module (or searcher) as a function of Ec/N0. Integration length is set to be 128 chip [8]. Simulation results closely agree with the experimental results of the implemented code acquisition module. In the experiment, we confirmed that when an appropriate integration length is selected, the detection probability of the implemented acquisition module is higher than 90% in the case of Ec/N0=-30 dB in AWGN channel environment.

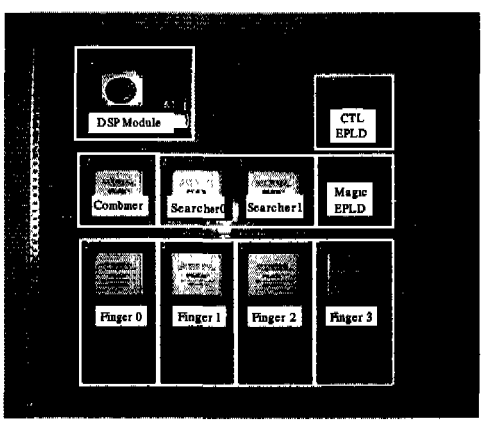
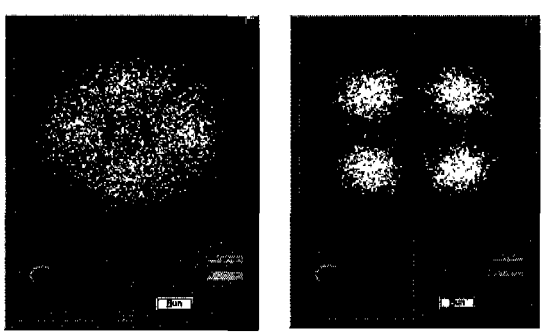


Fig. 7 Implemented BS demodulator card



(a) (b)

Fig. 8 Result of constellation measurement

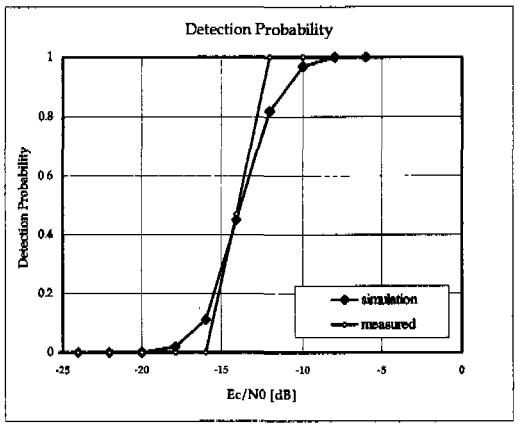


Fig. 9 Detection probability as a function of Ec/N0

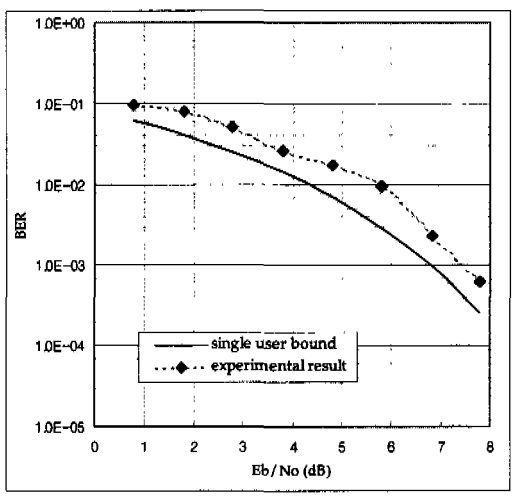


Fig. 10 BER performance as a function of Eb/N0

Figure 10 shows the bit error rate (BER) performance of the demodulator (or finger) as a function of Eb/N0. The solid line represents the theoretical bound in case of a single user [9], the dotted line represents experimental results of the implemented demodulator. The performance of the implemented demodulator is slightly worse (about 1 dB) than that of the theoretical results.

Also, in the field test of the system test plant shown in figure 1, we confirmed that the system equipped with implemented demodulator demonstrates good quality of wireless services, such as high quality speech, real-time video, and internet protocol (IP) based data services in a mobile radio environment.

V. CONCLUSION

In this paper, we described the issues on implementation and testing of wideband CDMA base station demodulator for the IMT-2000 STP based on cdma2000 RTT. The performance of the implemented base station demodulator is measured and compared with the theoretical performance bound. The STP equipped with this demodulator successfully provides wireless services such as high quality speech (9.6kbps), real-time video (384kbps) and internet protocol (IP) based data services (144kbps) under mobile radio environments.

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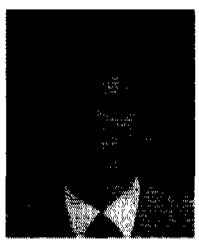

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