# TMS320F2812 DSP 칩을 이용한 30채널 텔레메트리 엔코더 구현

정회원 김 정 섭*, 장 명 진**, 시 광 규*

# Implementation of A 30-Channel PCM Telemetry Encoder with A TMS320F2812 DSP Chip

Jung-Sup Kim*, Myung-Jin Jang**, Kwang-Gyu Shi* ***Regular Members***

요 약

Artillery projectile에 장착될 PCM 텔레메트리 엔코더 개발에는 크게 세 가지 고려사항이 요구된다. 첫 번째는 샘플링률과 데이터 전송률과 같은 성능에 대한 것이다. 두 번째는 제한된 설치 공간에 따른 크기에 대한 것이고 마지막은 munition의 제한된 전원 공급에 따른 전력 소모에 대한 고려이다. 이러한 세 가지 조건에 맞는 해결책은 한 개의 칩으로 구현하는 것이다. 상용인 TMS320F2812 DSP 칩을 이용해서 프레임당 16채널 아날로그 데이터, 14채널 디지털 데이터와 2개의 프레임 동기 데이터를 랜더마이즈시켜 10Mbps 전송률로 송신하는 30채널 PCM 엔코더를 설계 구현하였다.

**Key Words** : Artillery projectile, TMS320F2812, PCM, PIE, EIC

ABSTRACT

There are three critical considerations in developing a PCM telemetry encoder to be installed in an artillery projectile. The first is the performance consideration, such as sampling rate and data transmission rate. The second is the size consideration due to the severely limited installation space in an artillery projectile and the last is the power consumption consideration due to limitations of the munition's power supply. To meet these three considerations, the best alternative is a one-chip solution. Using a commercially available TMS320F2812 DSP, we have implemented a 30-channel PCM telemetry encoder to process randomized data frames, composed of 16-channel analog data, 14-channel digital data and 2-frame synchronization channels per data frame at 10Mbps transmitting baud rate.

## Ⅰ. Introduction

The purpose of a telemetry system is to collect data at a place that is remote or inconvenient and to relay the data to a point where the data may be evaluated. Typically, telemetry systems are used in the testing of moving vehicles such as automobiles, aircraft, missiles, and artillery projectiles. Telemetry systems are a special set of communication systems[1]. Generally, telemetry systems are composed of the following six subsystems: data collection subsystem, multiplex subsystem, transmitter, receiver, demultiplex subsystem and data processor[1].

* 국방과학연구소4-1-3팀 ({jungsup, skg123}@add.re.kr), **국방과학연구소4-위성-4팀(mjin@add.re.kr)
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If the multiplex subsystem separates data in the time domain, it is referred to as a time division multiplex (TDM) subsystem. When we use a pulse code modulation (PCM) technique in a TDM subsystem, the TDM subsystem is called as a PCM telemetry encoder.

There are three critical considerations in developing a PCM telemetry encoder installed in an artillery projectile. The first is the performance consideration, such as sampling rate and data transmission rate. The second is the size consideration due to the severely limited installation space in an artillery projectile and the last one is the power consumption consideration due to limitations of the munition's power supply. To meet these three considerations, the best alternative is a one-chip solution.

As semiconductor technology progresses, there are many kinds of chips, such as micro-controllers, digital signal processors (DSPs), gate arrays and application specific integrated circuits (ASICs), available for a PCM telemetry encoder. By comparison, we could conclude that the DSPs were the most suitable chips in physical size, function, performance and developing flexibility. The TMS320F2812 was selected for the PCM telemetry encoder because of its high sampling rate, high operating speed and high transmission rate. Using a commercially available TMS320F2812 DSP, we have implemented a 30-channel PCM telemetry encoder to process randomized data frames, composed of 16-channels of analog data, 14-channels of digital data and 2-frame synchronization channels per data frame at 10Mbps transmitting baud rate.

## Ⅱ. TMS320F2812 DSP Structure

Fig. 1 shows the overall block diagram of the TMS320F2812. The TMS320F2812 has various modules to support its signal processing function. All modules can be categorized into three main groups: memory, control and peripheral. The memory group, consists of the flash memory, the single access RAMs (SARAMs), and the boot ROM. The control group contains the CPU, the timer and the system controller. The peripheral group includes the peripheral interrupt expansion (PIE), the external interrupt controller (EIC), the serial communication interfaces (SCIs), the serial peripheral interface(SPI), the multichannel buffered serial port (McBSP), the enhanced controller area network(ECAN), the event managers (EVA,EVB), the 12-bit analog-to-digital converter (ADC), and the mulptiplexed general-purpose input/output (GPIO). Of the various modules inside the TMS320F2812, the ADC, the SPI 0 and the McBSP module perform the main functions for implementing the 30-channel PCM encoder.

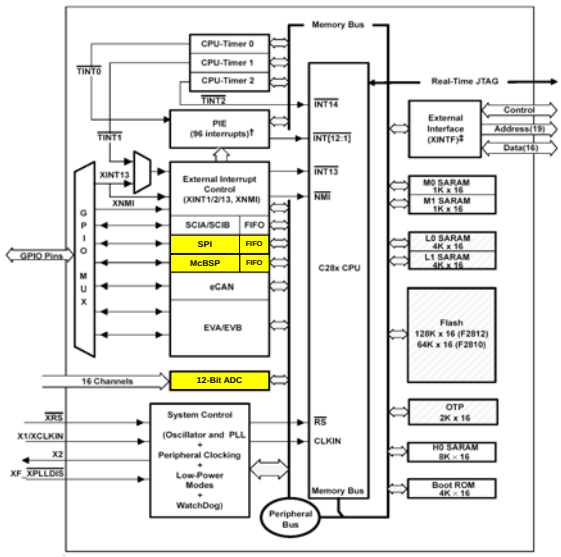



Fig. 1. Block Diagram of the TMS320F2812 [2]

### 2.1 Analog-to-Digital Converter(ADC) Module

Fig. 2 shows the block diagram of the ADC module. Analog signals are stored at the result registers after converting digital data through the analog MUX, the sample-and-hold(S/H) circuit, and the 12-bit ADC. The sequencer 1 and 2 controls the converting function as the value being set into the ADC control register. The 150MHz system clock is the ADC clock source and the high-speed pre-scaler divides the system clock. The output of the pre-scaler is used for the ADC clock.

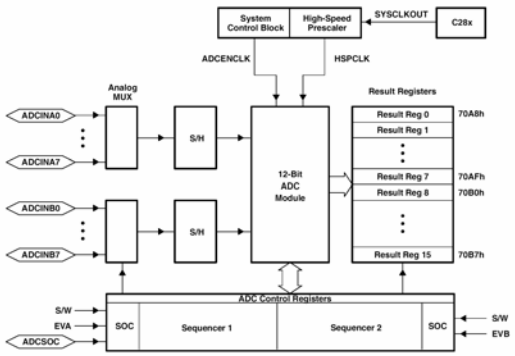



Fig. 2. Block Diagram of the ADC Module [3]

### 2.2 Multichannel Buffered Serial Port (McBSP) Module

Fig. 3 shows the block diagram of the McBSP module. The McBSP module is composed of a transmission port and a reception port. The transmission port of the McBSP module is only used for implementing the 4-channel PCM encoder. The McBSP module is further composed of the control register group and data register group. The control register group includes the McBSP control registers, multi-channel control registers and FIFO control registers.

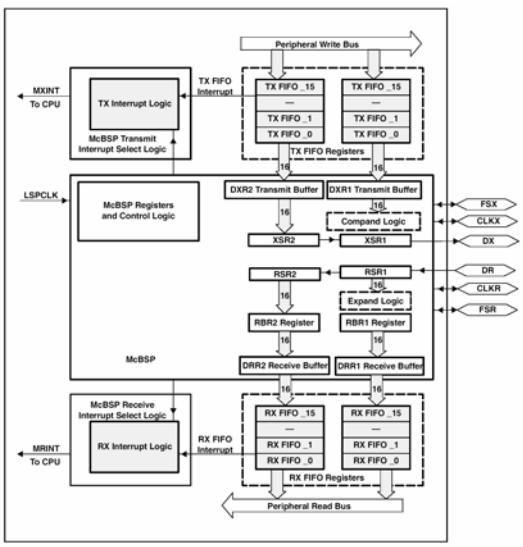



Fig. 3. McBSP Module With FIFO[4]

### 2.3 Serial Peripheral Interface(SPI) Module

Fig. 4 shows the block diagram of the SPI module. The SPI module has a high-speed synchronous serial input/output port. This allows a serial bit stream of programmed length(one to sixteen bits) to be shifted into and out of the device at a programmed transmission rate. Therefore, the SPI is normally used for digital serial communications between the DSP controller and external peripherals or another controllers. Even though the maximum SPI transmission rate is 37.5MHz, which decides digital channel receiving rate, we set SPI transmission rate to 10MHz.

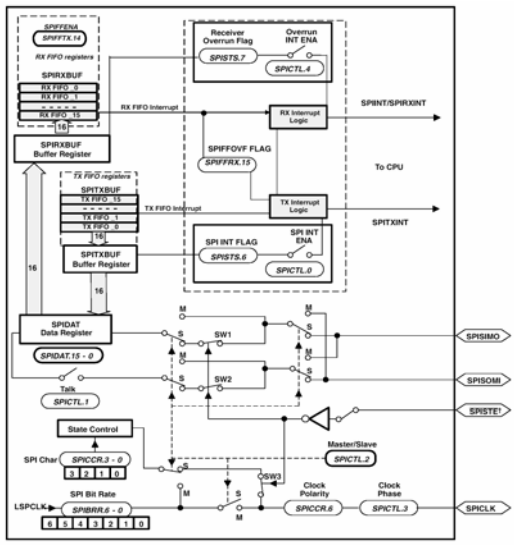



Fig. 4. SPI Module [5]

## Ⅲ. Design and Implementation

### 3.1 Output Format

To send various kinds of data at radio frequency in a PCM telemetry system, it is essential for source data to be formatted into a data frame. When many words are sent to the receiver, the data has to be composed in the sequence form as shown in Fig. 5. Without any sign of the start or end of the sequence, the receiver cannot recognize the start or end point of the sequence, and the receiver cannot decode the received data. Therefore, the frame synchronization data is essential to show the sequence start or

end point. This process can be handled in software and can be programmed in the DSP chip, so that a developer can implement any form of frame as long as the DSP hardware can support it. Fig. 5 shows the designed and implemented frame structure for the 30-channel PCM encoder, in which 16-analog channels, 14-digital channels and 2-frame synchronization channels. One frame consists of 32 words. The 16-analog channels are provided in parallel and 14-digital channels are provided in serial to the 30-channel PCM encoder. One word is composed of 16 bits. The data transmission rate and digital data receiving rate are 10MHz.

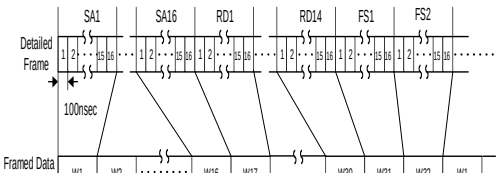



Fig. 5. Output Data Format of the 30-Channel PCM Encoder

## 3.2 Hardware Structure

As previously indicated, there are many modules in the TMS320F2812 DSP. Some of them are used for implementing the 30-channel PCM encoder. These are CPU, McBSP module, ADC module, SPI module, RAM, Flash memory and Clock. The CPU, ADC module, SPI and McBSP module are directly used for data processing such as sampling, receiving and transmitting data.

The other modules are used for supporting the operation of the ADC, the SPI and the McBSP. The operation of the encoder starts with the 16-analog inputs at the ADC and digital inputs at the SPI as shown at Fig. 6. The ADC module converts analog input data into digital data and saves it at RAM. The CPU formats these RAM data into frame data composed 32 words. The flash memory is used for loading and running the source code of the encoder. The clock module supplies the needed clock for the CPU. The McBSP transmits the framed data.

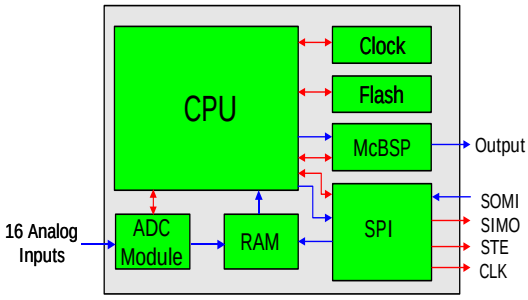



Fig. 6. 30-Channel Encoder Structure Embedded in the TMS320F2812

## 3.3 Software Structure

The main flow of the 30-channel PCM encoder software is shown in Fig. 7. When the system starts by power-on or system reset, the “Initialize System”service routine starts. This service routine initializes the system control registers, PLL, the system clock and so on. This service routine enables the SPI pins and McBSP pins to be added in the selection part of the GPIOs. The “Initialize SPI” service routine initializes the SPI control registers to the wanted state. At this routine, we can determine the SPI baud rate, Master/Slave selection and so on. The “Config & Start ADC” service routine enables the ADC module to start to convert analog signals into digital data. The “Set McBSP Control Registers” service routine initializes the McBSP control registers to the wanted state. At this routine, we can decide data transmission rate, frame length and so on. The “Start SPI Communication” service routine initiates SPI FIFO register transmission for serial data between the master and the slave processor. The master mode of the SPI module has to transmit one word to receive one word because the SPICLK signal is only active when the master has words to transmit. With 16-bit words, loading the first word with $8000_{16}$ means the MSB(Most Significant Bit) is a “1”. Since the SPI module transmit MSB first, this data bit can be used as the “Frame Synchronization” pulse over the SIMO pin. The last procedure that the SPI module performs, is loading the “dummy data” as zeros for the remaining 13-word period. The “Clear Input/

Output Registers" service routines resets all values of the randomizer registers.

In the "main loop", by branching to the "Get SPI Data" service routine, adapts the "polling method" instead of the "interrupt driven method". After loading 16 channels of analog data to RAM, done by "Load 16 Analog Conversion Words" service routine, the main program waits by polling the SPI RX FIFO interrupt flag. Once the number of words stored in the SPI RX FIFO registers is grater than or equal to the value of the RXFFIL bits(in this program, the value is 14), the main program not only sets the SPI RX FIFO interrupt flag to "1", it also accesses to the "Get SPI Data" service routine. When the "Get SPI Data" routine runs, it loads the SPI Rx FIFO registers into RAM. This function assumes that a global variable, named "Digital Offset", has been declared in the main function. "Digital Offset" servers to give the "Get SPI Data" routine a starting point in the array to begin loading the words from the SPI module. After adding two frame synchronization words to RAM, the "Randomizer" service routine activates before returning to the main program, if desired and the service routine clears the SPI RX FIFO interrupt flag in the SPI module.

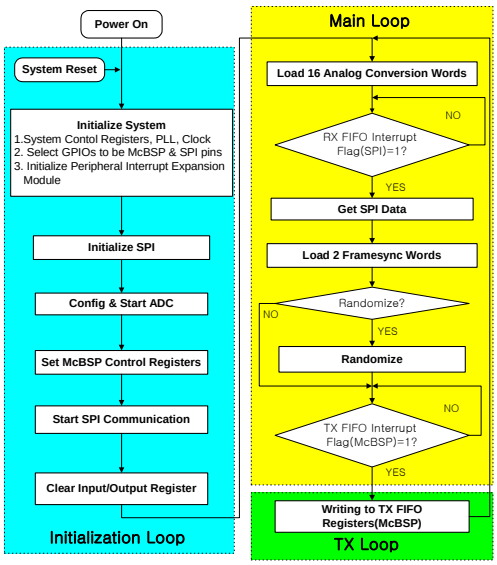



Fig. 7. Flowchart for the 30-Channel PCM Encoder Software

The "Randomizer" structure is shown in Fig. 8. It is composed of a shift register and module-2 adders(exclusive-OR gate). The output of the "Randomizer" is generated by the module-2 adding the framed data to the module-2 sum of the 14th and 15th stage output of the shift register. The output of the "randomizer" is also the input to the shift register. The "randomizer" is a very critical service routine for developing the 30-channel PCM encoder because it takes most of the CPU processing time. If the time for randomizing by the CPU is not coordinated with the time for the transmission by the McBSP module, transmission errors occur. Therefore, the processing time coordination between the CPU and the McBSP is the most important factor. The limitation CPU instruction cycles per frame of the "Randomizer" are about 7,200 CPU instruction cycles, If we design this "Randomizer" by using the "bit oriented technique", it takes about 16,000 CPU instruction cycles per frame. Therefore, the "Randomizer" was designed by adapting the "group oriented technique", requiring about 1,800 CPU instruction cycles per frame. In branching to the "Writing to TX FIFO Registers(McBSP)" service routine, located in the "TX Loop", we use the "polling method" instead of the "interrupt driven method". Once "the McBSP TXFIFO interrupt flag" has been set to "1", the main program branch to the "Writing TX FIFO Registers(McBSP)" service routine, loads the RAM data to the FIFO registers and clears "the McBSP TXFIFO interrupt flag". At this point, the program loops back to the start of the main loop, and will continue doing this, infinitely, until the encoder is turned off. For better performance, the "CODE_SECTION progma" to the "main loop"

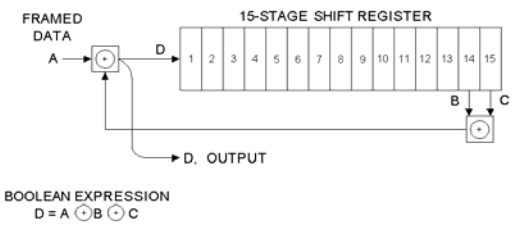



Fig. 8. "Randomizer" Structure[6]

and to the “writing McBSP TX FIFO function” was adapted.

## Ⅳ. Tests and Results

The implemented 30-channel PCM encoder test was performed using three types of tests. The first test was the loop back mode test, in which the analog channels are provided by the power supply and the digital channels are provided by the SPI module internally. The second test was the communication mode test, in which the analog channels are provided by the power supply and the digital channels are provided by the slave mode of the PCM encoder by using the other eZdsp board. As 14-digital channels are too long to see from the monitor of the logic analyzer, the test was performed with the 18-channel PCM encoder, composed of 2-digital channels. The last test was lab test, which was conducted by connection with the receiver composed of the bit synchronizer and decommutator. In this test, the analog channels are provided by the function generator and the digital channels are provided by the SPI module internally. The test setups are shown in Fig. 9, 10, 11.

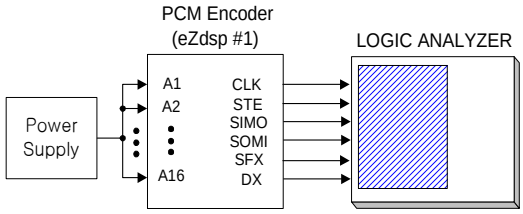



Fig. 9. The Loop Back Mode Test Setup

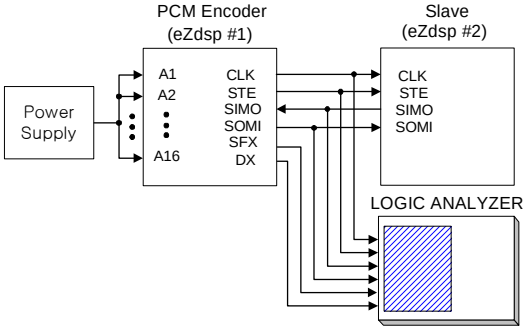



Fig. 10. The Communication Mode Test Setup

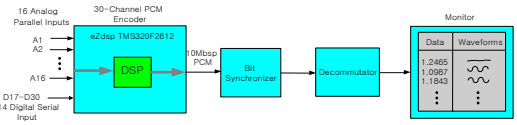



Fig. 11. The Lab Test Setup

Fig. 12 through Fig. 15 represent the output waveforms of the encoder. The output rate of the encoder is 10 Mbps, so one bit is 100 nsec duration. Also one channel period is 1.6μsec and

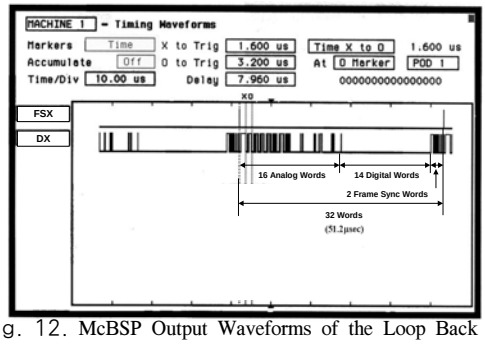
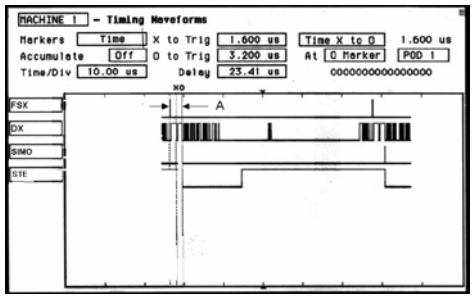
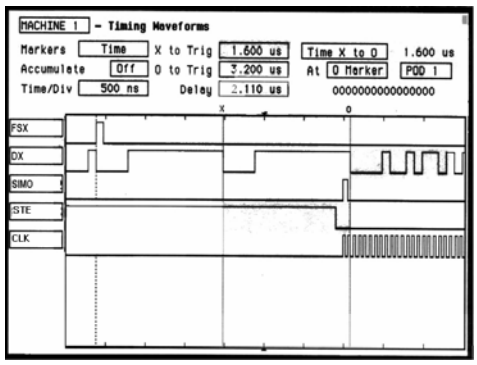



Fig. 12. McBSP Output Waveforms of the Loop Back Mode




(a)

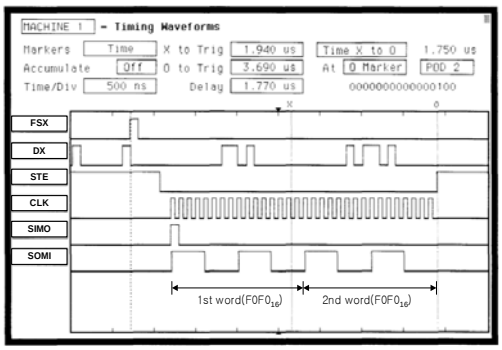



(b)

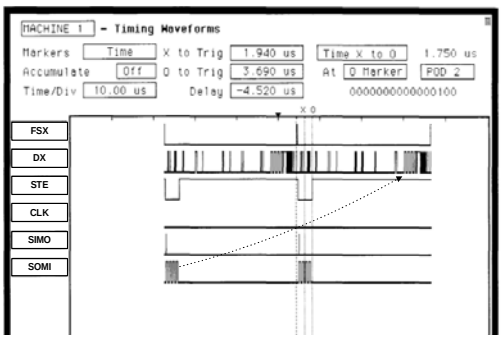
Fig. 13. McBSP and SPI Output Waveforms of the Loop Back Mode
(a) Zoom-in View
(b) Zoom-out View of the length “A”

one frame period is 51.2μsec, shown in Fig. 12. Fig. 12 and Fig. 13 are the output waveforms of the loop back mode, in the case of activating the randomizer and the derandomizer. The "FSX" and "DX" in Fig. 12 through 14 represent "transmission frame synchronization pulse" and "transmission data". The SIMO, STE and CLK represent "slave input master output data", "slave transmit enable signal" and "SPI clock signal". The left part of Fig. 13(a) shows, when the 3V signals are applied to the 1st and 2nd analog input ports, "DX", "SIMO" and "STE" pins are operating correctly. Fig. 13 (b) is enlargement of part "A" of the Fig. 13 (a) and it shows that the signals coming from the "DX", "SIMO", "STE", "CLK" pins are operating correctly.

Fig. 14 shows the communication moed output waveforms of the 18-channel PCM encoder at 10MHz SPI clock rate, in the case of activating the randomizer and the de-randomizer. Very short




(a)




(b)

Fig. 14. The Output Waveforms of the Communication Mode of the 18-channel PCM Encoder
(a) Focusing on SOMI
(b) Focusing on DX

single wires were connected between two eZdsp boards to avoid poor noise performance, which can easily happen in this single-ended transmission at high signaling rates.[7] Fig. 14 (a) shows that data is shifted in through the SOMI pin on the rising edge of the incoming CLK signal. The master mode performed its role satisfactorily. Fig. 14(b) indicates two digital words received from the slave can be transmitted through the DX pin.

Fig. 15 shows the output waveforms of the laboratory test, in the case of activating the randomizer and the de-randomizer. The recovered analog signals for the channel 1, 2, 8 and 16 are shown in Fig. 15 when the input signals are sine wave of 1500 mVp-p, 750 mVdc offset and 100Hz. This result shows that our 30-channel PCM encoder is performing correctly in a real test setup.

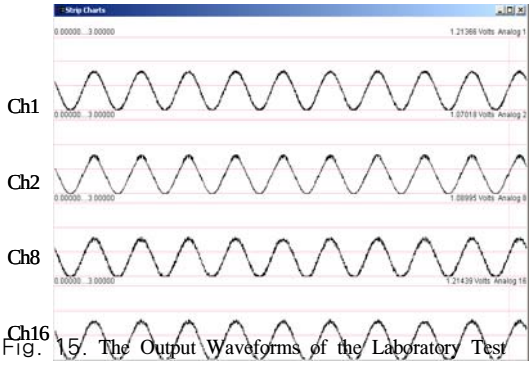



Fig. 15. The Output Waveforms of the Laboratory Test

## V. Conclusions

The PCM telemetry encoder is one of the important elements in a PCM telemetry system. The performance trend of a PCM telemetry encoder is changing to accommodation of a large number of channels and higher rates of speed transmission. Besides these improvements, there are size and power consumption considerations in developing a PCM telemetry encoder installed in an artillery projectile. To meet these considerations, the best alternative is the one-chip solution. A TMS320F2812 DSP was selected as a target device to develop a PCM telemetry encoder. The

30-channel PCM telemetry encoder was implemented by using the CPU, McBSP module, ADC module, SPI module, RAMs, and Flash memory in this DSP. The encoder has a data randomizer implemented by software. The randomizer plays an important role for transmitting secure information. It is very critical service routine in developing the 30-channel PCM encoder because it takes most of the CPU processing time. If the time for randomizing by the CPU is too long, and it is not coordinated with the time for the transmission by the McBSP module, transmission errors occur. We implemented a fast speed randomizer by adapting the "group=oriented technique". The performance of the 30-channel PCM telemetry encoder was verified through several tests.

## References


〔1〕 Frank Carden, Russell Jedlicka, "Telemetry Systems Engineering", Artech Inc., 2002.

〔2〕 Texas Instruments, "TMS320F2810, TMS320 F2811, TMS320F2812, TMS320C2810, TMS 320C2811, TMS320C2812 Digital Signal Processors Data Manual: SPRS174J", Texas Instruments, 2003.

〔3〕 Texas Instruments, "TMS320F28X Analog-to-Digital Converter (ADC) Reference Guide: SPRU060A", Texas Instruments, 2003.

〔4〕 Texas Instruments, "TMS320F28X Multi-channel Buffered Serial Port(McBSP) Reference Guide: SPRU061A", Texas Instruments, 2003.

〔5〕 Texas Instruments, "TMS320F28x System Control and Interrupts Peripheral Reference Guide: SPRU078A", Texas Instruments, 2003.

〔6〕 LORAL Data Systems, "PCM Training Course as Applied to Telemetry", LORAL Data Systems, 2003.

〔7〕 Texas Instruments, "Interfacing SPI and McBSP with Differential Interfacing Products: SLLA142", Texas Instruments, 2003.



**Jung-Sup Kim** *Regular Member*

1982-1986 received the B.S. degree in Electrical Engi- neering from Kyung -pook National University;

1986-1988received the M.S. degree in Electrical Engi- neering from Kyung -pook National University;

1995-2000 received the Ph..D. degree in Com-munication Engineering from Kyungpook National University;

1988-present Research fellow with Agency for Defense Development(ADD)

<*Research interests*> Spread Spectrum Communication, Satellite Communication, Software Defined Radio.

**Myung-Jin Jang** *Regular Member*

1982-1986 received the B.S. degree in Electrical Engi- neering from Kyung -pook National University;

1986-1988 received the M.S. degree in Electrical Engineering from Kyung -pook National University;

1988-present Research fellow with Agency for Defense Development(ADD)

<*Research interests*> Satellite Communication, Software Defined Radio.

**Kwang-Gyu Shi** *Regular Member*

1984-1988 received the B.S. degree in Electrical Engineering from Kyung-pook National University;

1988-2000 received the M.S. degree in Electrical Engineering from Kyung-pook National University;

2000-present Research fellow with Agency for Defense Development(ADD)

<*Research interests*> Signal Processing for Wireless Communications, Satellite Communication, Software Defined Radio.