40인치 고속 백플레인 채널에서 에러없이 40GbE 데이터 전송을 위한 적응 등화기

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An Adaptive Equalizer for Error Free 40GbE Data Transmission on 40 inch High-Speed Backplane Channel

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요 약

본 논문은 백플레인 채널을 통과하는 40 Gb/s 이상의 고속 신호 전송에 필요한 적응 등화기를 위한 구조와 알고리즘을 제안한다. 제안된 적응 DFE는 고속 수렴과 낮은 계산 복잡도를 갖는다. 40 Gb/s 시뮬레이션은 적응 등화기가 40 인치까지의 백플레인 스트립 라인을 위한 IEEE 802.3ba 요구사항을 만족하는 것을 보여준다.

Keywords : ISI, Adaptive Equalizer, Backplane, DFE

ABSTRACT

This paper proposes the structures and algorithms for the adaptive equalizer that are required to allow high speed signaling over 40 Gb/s across a backplane channel. The proposed adaptive DFE has a fast convergence and low computational complexity. Simulations with a 40 Gb/s show that our adaptive equalizer can meet the IEEE 802.3ba requirement for backplane strip line up to 40 inches.

Ⅰ. Introduction

According to IEEE 802.3ba, the 40 Gb/s high speed Ethernet backplane is provided as the 4 channel 10 Gb/s. It requires performance that complies with 10^{-12} BER while the data is transmitted via a 40 inch, 4-layer fire-resistant (FR-4) backplane strip line. When the data is transmitted via the high-speed telecommunication channel, the channel is frequently distorted and random noise flows into the transmission signal. Consequently, the loss in the channel causes ISI (Inter Symbol Interference) to neighboring channels. If ISI is not compensated, it can cause a high error rate or bit detection error, which can limit the maximum distance and data rate. Therefore, the adaptive equalization technique is required indispensably, which restores the original signal by compensating for the characteristics of the ever-changing channel at the receiving end, in order to remove ISI caused by the channel and to provide 10^{-12} bit error rate (BER) on 40 inch FR-4 backplane for the 40 Gb/s Ethernet channel[1-4].

To reconstruct the transmitted signal, the receiver must compensate for the channel distortion and minimize the impact of the channel noise. Such

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compensation is called equalization, and it is at the heart of most communication systems. A method to remove the ISI caused by the channel is to apply the equalizer at the receiver. The merit of including receiver equalization is that the equalizer parameters can be adjusted by measuring the quality of the incoming signal to compensate for the process and temperature variation of the signal propagation medium.

The major objective of this paper is to develop a standard-based receive adaptive equalizer that conforms to 40 Gb/s Ethernet.

Ⅱ. Characteristics of Backplane Channel for 40 Gb/s

The strip line structure for 40 inch backplane was designed for the 50 ohm differential pair as shown in Figure 1, using the Computer Simulation Technology Microwave studio (CST MWS) tool (PCB impedance and capacitance calculator). By observing this structure, we need to know how much attenuation can be obtained from the 4 lane backplane channel, compared with the existing single lane backplane channel.

Figure 2 shows the insertion loss measured against the backplane channel that was designed using a 3D CST tool. The variation of the insertion loss by backplane trace is simulated for the channel S-parameter. The result of simulation that measured the insertion loss against the backplane trace length shows that the degree of channel attenuation by frequency increases as the frequency increases.

Attenuation of the insertion loss increases as the backplane trace length increases. Signal attenuation includes the degree of attenuation in all media areas

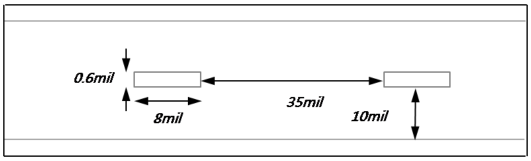

Fig.1. Designed 40 inch backplane strip line structure

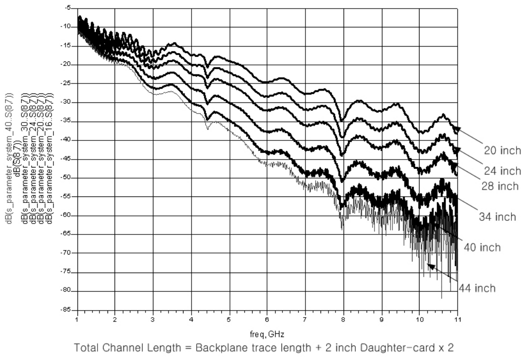

Fig. 2. Attenuation characteristics by FR-4 backplane strip line length according to the frequency

(trace, connector, package, pad, etc.) As this signal contains the cross talk element, regular attenuation is not observed.

To verify the insertion loss measurement result of a 10 Gb/s, 34 inch backplane channel indirectly, it was compared with the channel insertion loss of the 34 inch backplane system, which was used for the 6.25 Gb/s DFE design. The result has shown that the attenuation characteristics of each frequency were similar. Regarding the entire backplane channel, over 56 dB was observed even though it is one pair. The 4 pair, 34 inch backplane channel with the proposed structure has shown 51 ~ 53 dB attenuation. It was found that the pulse response measured at 40 inch backplane channel with the proposed structure has a relatively higher value (peak-to-peak) at 10 Gb/s than the one measured at 34 inch backplane channel.

It was also found that the insertion loss of the backplane channel having a 40 inch strip line is affected more by the channel length, because its length is longer than 34 inches. And, it provided a better result than the 56 inch channel that has longer channel distance relatively[5].

Figure 3 shows the output pulse response of 46 inch backplane channel. The simulation condition was to supply the pulse having a 1 volt peak (input peak a=0.6GHz, b=5,300).

As shown in Figure 3, other values exist near the maximum value shown m15, which becomes the pre

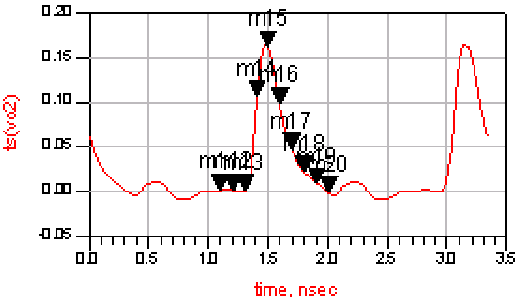

Fig. 3. Pulse response of 46 inch backplane channel

-cursor and post-cursor value in the pulse response. Using the result value of those pulse responses, the system channel response is modeled to compensate for the pre-cursor or post-cursor value. Based on the simulation result, the adaptive equalizer is designed for 40 GbE that has a 40 inch trace.

The system model was configured to estimate the channel. The configured channel model was 40 inch backplane trace, and daughter card, connector, and pad that were configured in 4 inches in total. The channel component was figured out, using the impulse response of the channel that has been configured in this way. The channel component exists at the front and rear end around the cursor, which is the on-time sample. When the channel component exists at the front end, it is called “pre-cursor”. It is called “post-cursor” if it exists at the rear end. These components affect the data transmission process, and act as an ISI component.

In this paper, 0.1 ns was set as the time interval, and total 6 samples were set as the channel response value (2 samples for the pre cursor component, 3 samples for the post cursor component, and 1 sample for the cursor), in order to perform system simulation.

Figure 4 shows the impulse response of defined channels (0.1 ns interval). Figure 5 shows the values at the frequency reign for the response sample of the defined channel.

The impulse response becomes asymmetrical due to group delay distortion and the resulting long tail of the impulse response causes more severe post-cursor ISI, which furthermore degrades the far-end

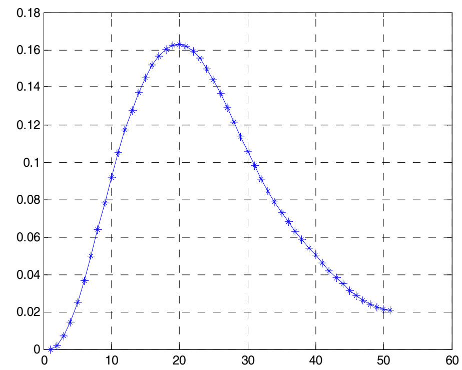

Fig. 4. Impulse response of defined characteristics (0.1 ns interval). X axis is sample, Y axis is response of channel

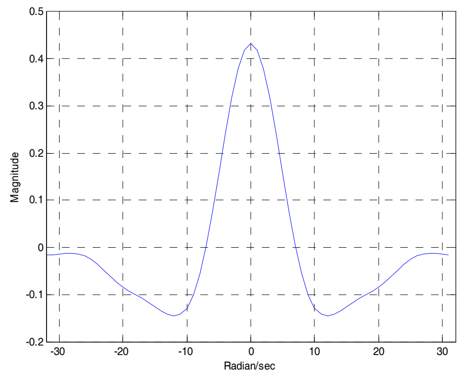

Fig. 5. values at the frequency region for the response sample of the defined channel

eye opening. From the pulse response of the channel, it is also observed that the optimal tap number obtained through Sign-Regressor least mean square LMS optimization is close to the least number of symbol-spaced points that cover the greater part of the tail of the pulse response. Therefore, the tap number of an FIR filter can be optimized in terms of performance and complexity trade-off of implementation

Ⅲ. An Adaptive Equalizer for Error Free 40 GbE Data Transmission on 40 inch High Speed Backplane Channel

3.1 Structure of Adaptive Equalizer

Once the system responses are known, we can use them to design the receiver, including decision feedback equalizer. The feed-forward filter (FFF) and decision feedback equalizer (DFE) can be considered as an adaptive equalizer. The FFE allows less complex hardware but uses big volt swing and design flexibility of the fixed tap coefficient is small when the channel is changed[4]. DFE is the most common nonlinear equalizer with quite low complexity, fast convergence time, and good tracking capacity. DFE is one of the most effective approaches to eliminate the ISI by using past symbols interfering with the currently transmitted symbol. A new DFE equalizer for the 40 GbE backplane channel IEEE 802.3ba is proposed.

It's DFE, whose structure closely resembles an infinite impulse response (IIR) type filter. Like the linear transversal equalizer, it contains a tapped delay line that sums weighted versions of past symbols. In order to properly utilize the feedback data, the tap weights must be chosen correctly to match the distortion of the previous symbols.

Figure 6 shows the proposal of the DFE structure where the FFF is removed. Sign-Regressor LMS algorithm was used in the proposed structure for an error calculation and tap coefficient application. Something new in this structure is to calculate error distribution and to use it in a tap coefficient application. If the current error is used, the system converges and disperses abnormally depending on the step size, because the difference between the detector's output value and input value should be small that is caused by channel attenuation but it is not actually small. Due to its relative simplicity of implementation, the LMS algorithm and its variants are the most commonly used in receive end equalizers[3].

Therefore, error distribution is used to acquire the optimal value at the system convergence sector, and the tap coefficient is determined using error distribution.

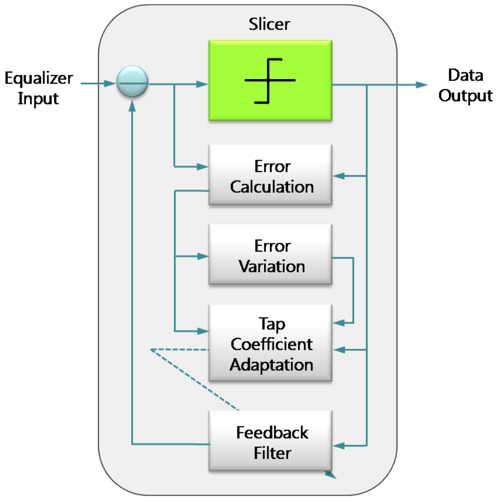

Fig. 6. Structure of proposed adaptive equalizer

3.2 Adaptive Algorithm

Figure 7 shows DFE convergence, and the 10 Gb/s PAM-2 signal was used on a 40 inch FR-4 backplane.

Equalizer tap coefficient application algorithm is Sign- Regressor LMS algorithm, since the detector output is used. Let's assume that the current LMS algorithm is described by the expression (1).

$$W_{k+1} = W_k + \mu(-\nabla_k) = W_k + \mu e_k X_k \quad (1)$$

As described in the expression (1), ˉ in LMS algorithm becomes the data input value. However, Sign-Regressor LMS algorithm doesn't use the data value ˉ without modification. Instead, the result of applying sign function to this value is used. As a result, it can be described as the expression (2).

$$W_{k+1} = W_k + \mu e_k sgn(X_k) \quad (2)$$

The error that corresponds to each value in the expression 2 can be described as the expression (3).

$$e_k = \text{sgn}(X_k) - X_k \quad (3)$$

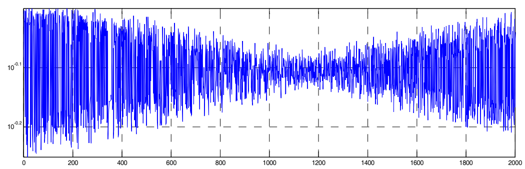

Fig. 7. Error convergence of 5 tap DFE

As the expression describes, the error value is acquired by comparing it with 1 and -1.

The e_k error value increases, because the receiving signal level is small. Therefore, convergence is made at some parts as shown in Figure 7 but the error value is not actually converged completely. That is, the equalizer configured solely of feedback filter (FBF) has the structure problem as shown in Figure 6.

Consequently, the accurate data can be obtained only when the tap coefficient value is calculate at the sector where the error value is minimal and maximum eye opening can be obtained. The system needs to have an algorithm that allows a minimal error value, in order to reduce those errors.

To make the algorithm that obtains a minimal error value, the tap coefficient value is fixed in this study, using the variance of the absolute error value. As the variance at the sector where the value becomes minimal is the smallest one, the corresponding value is expressed. The expression (4) and (5) describes it.

$$M_e = \frac{1}{N}\sum_{k=1}^{N}(\mathrm{sgn}(X_k) - X_k)^2 = \frac{1}{N}\sum_{k=1}^{N} e_k^{\,2} \qquad (4)$$

$$V_e = \frac{1}{N}\sum_{k=1}^{N}(e^2 - M_e)^2 \qquad (5)$$

When error distribution is calculated using this expression (4), and (5), the result as shown in Figure 8 can be obtained. As we can see in the figure 8, the minimum value of error distribution can be obtained in 19 ~ 20 times index. Therefore, the tap coefficient can be decided at the minimum error distribution sector, and performance can be obtained using the tap coefficient.

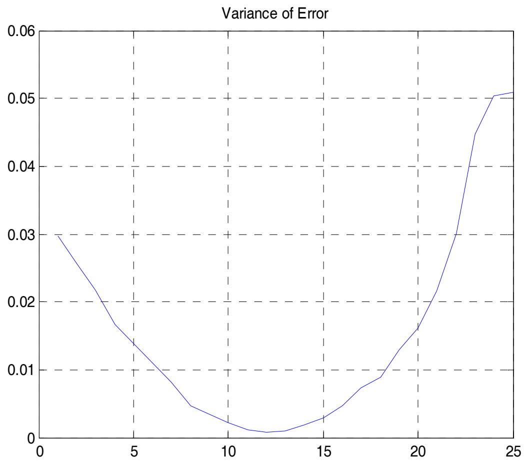

Fig. 8. Distribution of absolute error values

Ⅳ. Simulation Results and Discussion

The pattern generator uses a pseudorandom bit sequence (PRBS) with the length of 27^{-1}. A normalized 1 V_{pp} PRBS 2^{11}-1 data sequence was transmitted at 10 Gb/s through the channel. The pattern generator itself has a peak-to-peak jitter of approximately 10 ps.

A conventional 3 post tap equalizer was applied as transmitter pre equalizer. Simulations have been performance using the proposed method, and the 2/4 -PAM signaling method, respectively, with the adjustment of LMS error deviation points. A Matlab program is then used to optimize finite impulse response (FIR) filter coefficients. We evaluate the performance of the adaptive equalizer in the presence of crosstalk on each channel of the 40 Gb/s Ethernet communication system consisting of 4 channels capable of 10 Gb/s per channel. This equalizer is to apply to the receive system. Figure 9 shows the eye diagram where 2-PAM signals pass through the channel.

As shown in Figure 9, the channel should go through an extremely poor channel environment, and the eye is closed due to channel ISI. Therefore, the transmitter pre-equalizer distorts the value in advance so that the signal with a relatively small ISI can be obtained at the receiving end when the signal passes through the channel. In this study, the channel was pre-compensated using a 5 tap transmitter pre-equalizer at the sending end. Figure 10 shows the result of channel compensation.

2-PAM results is used 5 tap pre transmitted equalizer with FBF equalizer at receiver. Figure 11 shows the eye diagram that is obtained after passing through the adaptive equalizer after receiving the signal, using the Sign-Regressor algorithm intro-

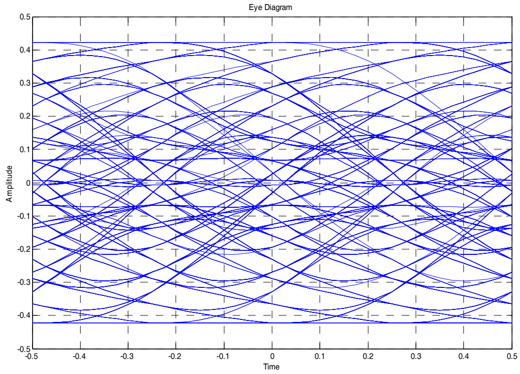

Fig. 9. 2 PAM signal's eye diagram after passing through the channel

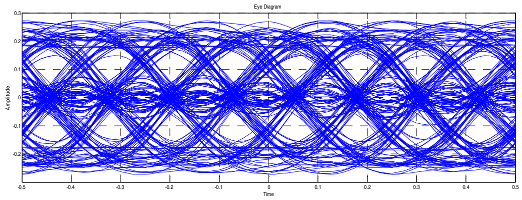

Fig. 10. 2 PAM signal's eye diagram after passing through the channel via the 5 tap's transmitter pre-equalizer

duced above. When the 5 tap DFE was used, opening eye described in Figure 11 could be obtained.

Duo-binary and 4-PAM (pulse amplitude modulation) signal is used for equalizer consisting of 1 tap FFF and 5 tap FBF as receiver equalizer with 3 tap transmitter pre-equalizer. Figure 12 and 13 shows the opening eye diagram that is obtained after passing through the receive equalizer after receiving the 4-PAM and duo-binary signal under the same condition as 2-PAM signal introduced above.

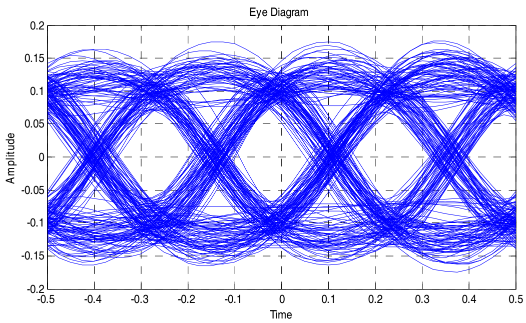

Fig. 11. 2 PAM signal's eye diagram of passing through the DFE that is computed of 5 tap

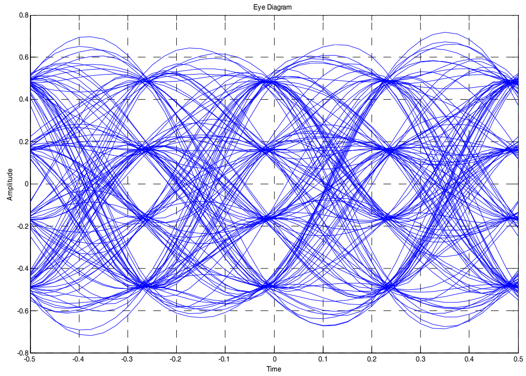

Fig. 12. 4 PAM signal's eye diagram of passing through the DFE that is computed of 1 tap FFF, and 5 tap FBF via the transmitter 3 tap Pre-equalizer

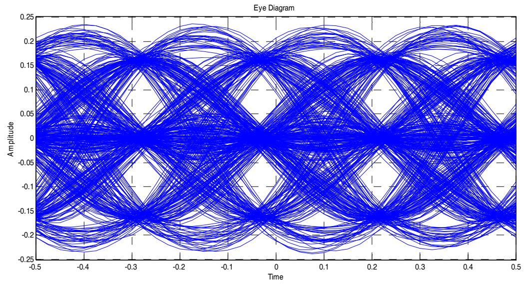

Fig. 13. Duo binary signal's eye diagram of passing through the DFE that is computed of 1 tap FFF, and 5 tap FBF via the 3 tap transmitter Pre-equalizer

Ⅴ. Conclusion

This paper designed a 40 inch FR-4 backplane transmission channel, and proposed the adaptive equalizer structure and Sign-Regressor LMS algorithm based on it, in order to implement adaptive equalization at the receiving end of the backplane channel. For 40 Gb/s high-speed data communications pass through the backplane, a 10 Gb/s 4 channel adaptive equalizer with DFE except for FFE was designed and simulated.

The proposed adaptive DFE has a fast convergence and low computational complexity. Simulations with a 40 Gb/s show that our adaptive equalizer can meet the IEEE 802.3ba requirement for backplane strip line up to 40 inches.

Proposed DFE meets the requirements of the IEEE P802.3ba standard-based adaptive equalizer to implement equalizers on the receive end of a backplane channel.

The eye of the channel is closed when it passes through the poor channel environment due to ISI. At this time, the adaptive equalizer measures the quality of the incoming signal to the channel, and adjusts equalizer parameters to compensate for channel conditions or temperature changes of the signal propagation media, so that the 40 Gb/s Ethernet system can be robust against channel intervention and channel jitter.

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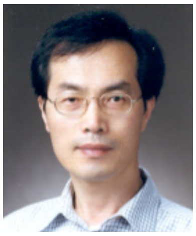

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