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WPON 응용을 위한 고속 CMOS어레이 광트랜스미터

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A High Speed CMOS Arrayed Optical Transmitter for WPON Applications

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요 약

본 논문은 멀티 채널의 어레이 집적 모듈을 갖는 광트랜시버를 위한 2.5 Gbps 어레이 VCSEL driver의 설계 및 구현에 관한 것이다. 본 논문에서는 광트랜시버에 적용된 1550 nm high speed VCSEL을 드라이브하기 위하여 0.18 μm CMOS 공정 기술을 이용하여 자동 광전력제어 기능을 갖는 2.5 Gbps VCSEL (수직 공진기 표면 방출 레이저) 드라이버 어레이를 구현하였다. 광트랜스미터의 폭넓은 대역폭 향상을 위해 2.5 Gbps VCSEL Driver에 네가티브 용량성 보상을 갖는 능동 궤환 증폭기 회로를 채용한 결과 기존 토폴로지에 비해 대역폭, 전압 이득 및 동작 안정성의 뚜렷한 향상을 보였다. 4채널 칩은 최대 변조 및 바이어스 전류하에서 1.8V/3.3V 공급에서 140 mW의 DC 전력만 소모하고, 다이 면적은 기존 본딩 패드를 포함하여 850 μm × 1,690 μm를 갖는다.

Key Words : WPON, CMOS, arrayed VCSEL Driver, ABC, AMC

ABSTRACT

In this paper, the design and layout of a 2.5 Gbps arrayed VCSEL driver for optical transceiver having arrayed multi-channel of integrating module is confirmed. In this paper, a 4 channel 2.5 Gbps VCSEL (vertical cavity surface emitting laser) driver array with automatic optical power control is implemented using 0.18 μm CMOS process technology that drives a 1550 μm high speed VCSEL used in optical transceiver. To enhance the bandwidth of the optical transmitter, active feedback amplifier with negative capacitance compensation is exploited. We report a distinct improvement in bandwidth, voltage gain and operation stability at 2.5Gbps data rate in comparison with existing topology. The 4-CH chip consumes only 140 mW of DC power at a single 1.8V supply under the maximum modulation and bias currents, and occupies the die area of 850 μm × 1,690 μm excluding bonding pads.

Ⅰ. Introduction

Recently, the demands for high rate access network services has been rapidly increasing and stimulating the development of economical optical access system. For fiber-to-the- home applications enabling high rate data lines to individual homes, economical PON (Passive Optical Network) system becomes most native technology.

In low-cost and high volume short-haul applications around several Gbps optical transmitter for WPON, commercial CMOS

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technology has been of interest and a good candidate for implementing the VCSEL driver. This is because CMOS technology can offer high yield and high degree of integration, leading to low cost and low power. Therefore, the objective of this paper is to investigate the possibility of implementing a high-speed CMOS VCSEL driver for these cost sensitive applications. In this paper, the design of 2.5 Gbps CMOS VCSEL driver array type is reported in 0.18-μm CMOS process with high performance at low cost and low power consumption.

In this paper, a 4 channel VCSEL driver array with analog optical power control is designed and implemented in 0.18 μm CMOS technology. Section II describes the design details of the proposed VCSEL driver, especially ABC (automatic bias control) and AMC (automatic modulation control) schemes. In section III, the simulation results will be presented and analyzed. Finally, the conclusion is given by section IV.

Ⅱ. Proposed VCSEL Driver

In this paper, The General requirements[1] for the VCSEL driver to be used in WPON are summarized in Table 1. and a 4 channel VCSEL driver array[2-4] with analog optical power control shown in Figure 1 is designed and implemented in 0.18 μm CMOS technology.

표 1. VCSEL driver 일반 규격
Table 1. General specification of VCSEL driver

Specifications	Single channel 2.5 Gbps	4 channels 5 Gbps	4 channels 10 Gbps
Technology	0.18 μmCMOS Process	0.13 μm CMOS Process	0.13 μm CMOS Process
Data rate (Gbps)	2.5	5	10
Bandwidth(GHz)	2.5	5	10
Voltage gain(dB)	-	10	10
Ibias(mA)	-	4	20
Imod(mA)	-	13	20
Supply voltage	core 1.8 Vdc, I/O 3.3 Vdc	core 1.8Vdc, I/O 3.3Vdc	core 1.8 Vdc, I/O 3.3 Vdc
Power Dissipation	24 mW	1025 μV	374 mW
Chip size (μm²)	960 × 750	1,740 × 1,500	2,050 × 830

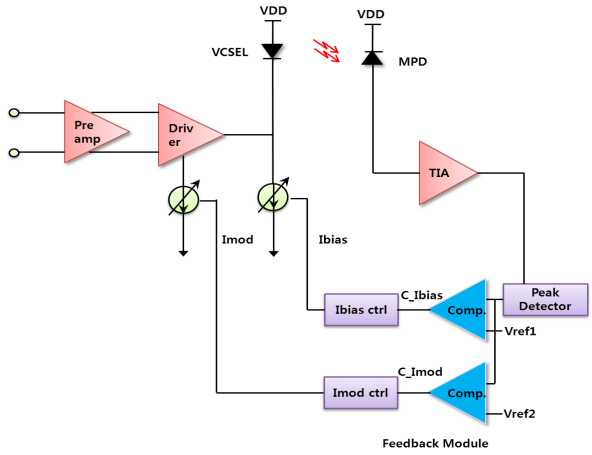


그림 1. 제안된 VCSEL driver 회로도.
Fig. 1. Schematic of the proposed VCSEL driver.

Fig. 1 shows the proposed VCSEL driver with adaptive optical power control. Designed VCSEL driver consists of input buffer, pre driver, main driver and ABC/AMC[5] blocks. Imod represents the modulation current of VCSEL, corresponding to the optical output swing range, whereas Ibias is the bias current of VCSEL which corresponds to the norminal threshol current , I guarantees that the VCSEL operates idealy. The Input is designed to cover both LVDS and CML input signals. A VCSEL and monitoring photodiode (MPD) are externally implemented for the verification ABC/AMC schemes.

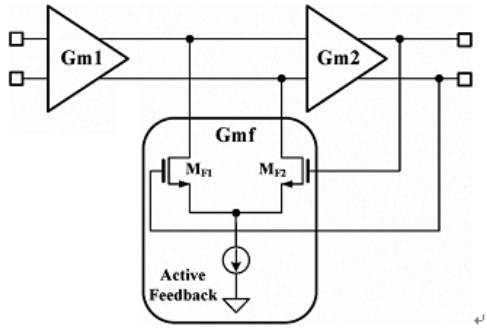


그림 2. 네가티브 임피던스 보상을 갖는 능동 피드백 드라이버 회로.
Fig. 2. Schematic of Active Feedback Pre Driver with Negative Impedance Compensation.

2.1. Pre-driver Design

Pre driver is designed using active feedback amplifier with negative compensation. we proposed a pre driver using active feedback and negative impedance compensation as shown in Figure 2. Active feedback between two common-source amplifiers can improve gain-bandwidth product of the amplifier. The active feedback between two transconductance stages can enhance the total bandwidth of limiting amplifier. However, intermediate node between two common source stages very capacitive. To compensate this parasitic capacitance, feedback stage is added at that point.

In the case of the register load, it has better bandwidth characteristics and linearity than a current load using an MOS. If the resistor load had a tuning function for a power constraint, and the optimum value fitting the input swing is chosen, radical changes in the bandwidth characteristics can be controlled to a certain degree. We lowered the load resistor value to restrain the overshooting caused by the Miller capacitor. To stabilize the operation of the VCSEL, we used 3.3V. And since the used transistor was 1.8V, we adopted a cascode structure considering an overload.

Figure 3 shows the simulated AFB (active feedback) frequency response of the pre driver with and without active feedback. Simulation results verify that the active feedback technique has 59% of bandwidth enhancement from 1st and 3rd curve.

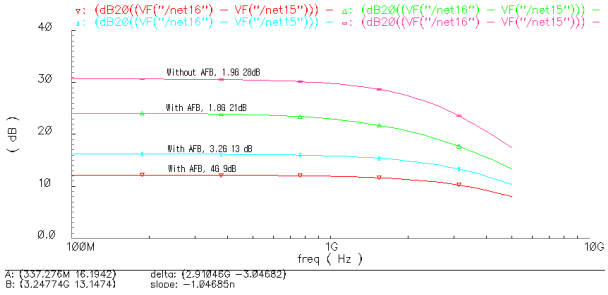


그림 3. 프리 드라이버의 AFB 응답 시뮬레이션.
Fig. 3. Simulated AFB Response of Pre Driver.

2.2. Main Driver Design

The function of the main driver is to offer enough current to drive a VCSEL. Figure 4 shows a block diagram of the main driver used for the optical transmitter architecture in this research. We present a new scheme of ABC and AMC for arrayed multichannel VCSEL driver. It is formed with a switch block for controlling the bias to control the reference current value, a block for Ibias and Imod, each with four switches. To offer sufficient current to a VCSEL, the circuit was designed to produce both Imod and Ibias, combine two bias signals output from the differential amplifier, and at the same time, increase the output resistor value. With this circuit, we can guarantee a high voltage gain. Since a MOSFET has no current that flows into the gates, if a multistage cascode is connected, a high output resistor can be obtained, which increases the frequency characteristic and guarantees a flexible output swing of the driver. After a 3-bits control signal (Vref 1, 2, and 3) is produced following the size of the input signal of the TIA (transimpedance amplifier), the input signal is compared to each Vref and the control signal is determined. The bias current is controlled using several PMOS paths, and modulation current control is set to change the bias of the transistor. As shown in Figure 2, we arranged four or five PMOSs in a row, and then controlled the bias by turning on or off each PMOS. For the modulation current, we arranged four or five bias transistors into which Vb is input, and controlled the current by turning on or off each transistor. These control signals in the desired range are transferred through a feedback loop.

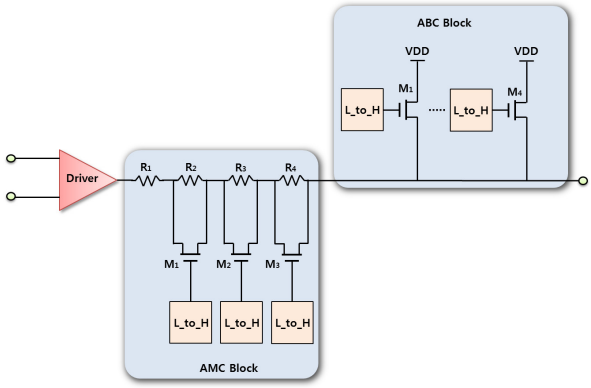
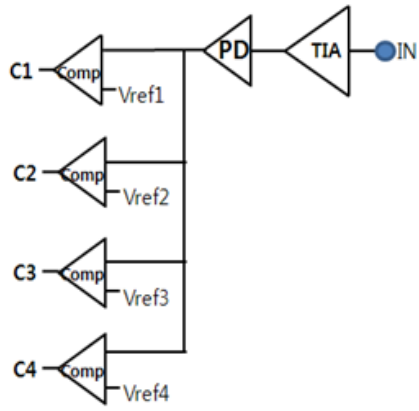
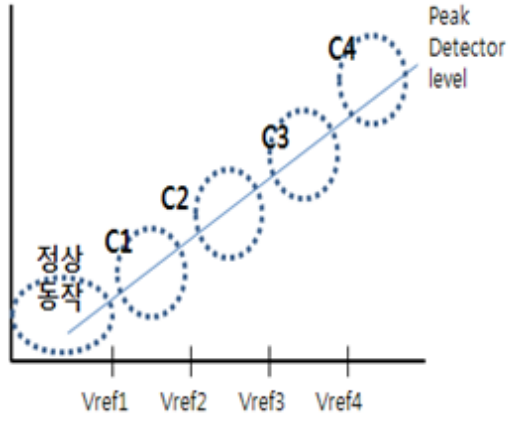


그림 4. ABC 및 AMC를 갖는 메인 드라이버
Fig. 4. Main Driver with ABC and AMC.



(a) 제어신호 발생
(a) Generation of the control signal



(b) 제어신호의 결정
(b) Decision of the control signal.

그림 5. ABC 및 AMC를 갖는 제어.
Fig. 5. Control with ABC and AMC.

In order to compensate the temperature dependency of the VCSEL, peak comparator circuits including AMC (automatic modulation control) and ABC (automatic bias control) from a monitoring photodiode are implemented. If the temperature of the VCSEL increases, the operating point of the VCSEL moves based on the bias control and a flattening function of the optical power is implemented. In this architecture, once the reference voltages of the AMC and ABC circuits are determined at the outside, the initial bias and modulation currents for the stable optical power of the VCSEL are automatically installed. For the given reference voltages, as temperature increases the lower monitoring photodiode current is fed into the TIA due to the decreased transmitted optical power of the VCSEL. In the next turn, the increased bias and modulation currents rather decrease the output voltage level of the peak detection circuits. Therefore, the proposed optical transmitter can provide stable performances over a wide temperature. To control the current variation in more detail, the gap between the Vrefs can be narrowed using several comparators.

As shown in (a) of Figure 5, after the TIA receives the output of the VCSEL through the PD (photo diode), the peak of the output current is detected, is then compared to the reference voltage, and a control signal is produced. As shown in (b) of Figure 5, the control signal varies depending on in which range of the reference voltage the detected peak is within. We measured the data for this in advance and set the Vref values. If necessary, more than 4 bits can be additionally increased. In continuous mode, the ABC and AMC function simply performed by

adjusting the laser current until the average PD current reaches a desired value. For burst mode, the average PD current is not a suitable control variable.

Ⅲ. LAYOUT & Measurement RESULTS

Fig. 6 shows layout of the final 4channels VCSEL driver. As shown in the figure, the connection of an electrostatic discharge (ESD) interacts with the speed and characteristics of the ESD[6]. If an ESD is connected to the ground, it is protected but the speed is diminished. The chip layout of 4 channel 2.5 Gbps VCSEL driver array[7] is shown fabricated by TSMC (Taiwan Semiconductor Manufacturing Company). in Fig. 7. For the top metal, metal 6 is used, and for Mim cap, 1.5 fF/sq is utilized. For the inductor, a thick metal was used to achieve a high Q. Using a high R reduces the resistance area through 1kΩ /sq. The VCSEL channel pitch is 250 μm with direct connections to the laser's cathods at conntact pads around the periphery of the array chip.

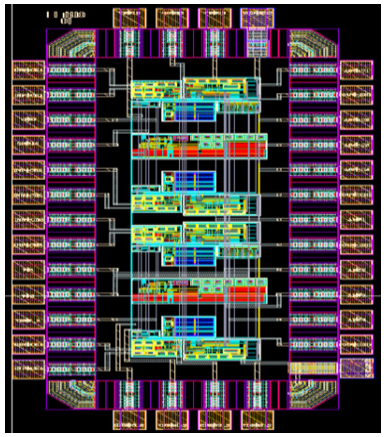


그림 6. 칩 레이아웃.
Fig. 6. Chip Layout..

Pre driver is designed using active feedback amplifier with negative compensation. Figure 8 show the simulated S-parameter patterns with auto-modulation control and auto-bias control. We from the simulated S-parameter, can see the

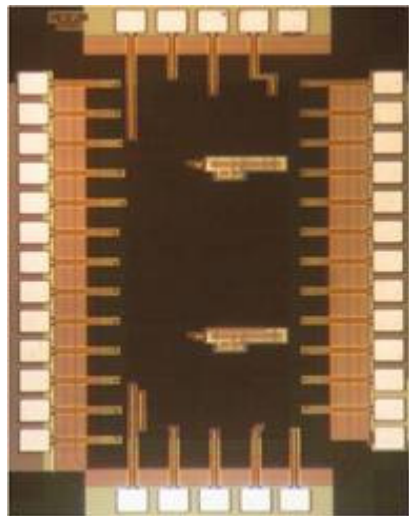


그림 7. 4 채널 2.5Gbps VCSEL Driver 칩.
Fig. 7. 4-channels 2.5Gbps VCSEL Driver Chip.

bandwidth and gain. After the matching of the output impedance, we measured the S-parameter to see the bandwidth and gain. The results of measuring I/O characteristics show that the pre-driver can be treated with a very large input swing of up to 400 mV. The results of measuring the performances of the AMC and ABC show that it has a satisfactory bandwidth of 2.5 GHz. From an S-parameter simulation for the gain, the design value of the gain was about 1dB and its measurement value was between －12.6 dB and －7.8 dB. The difference between the design value and the measurement value is therefore between 13.6 dB and 8.8 dB. It seems that a loss occurred when they were connected on the board. In the measurement of the Tx, the gain does not have a significant effect on the performance, but was measured to be lower than the design value. It was determined that the most important thing is that a VCSEL is made to be driven to some degree when measuring the optical characteristics. S11 was measured to be about －6 dB; and S22, less than －15 dB. Thus, this shows that the output impedance was designed to match 50 Ω.

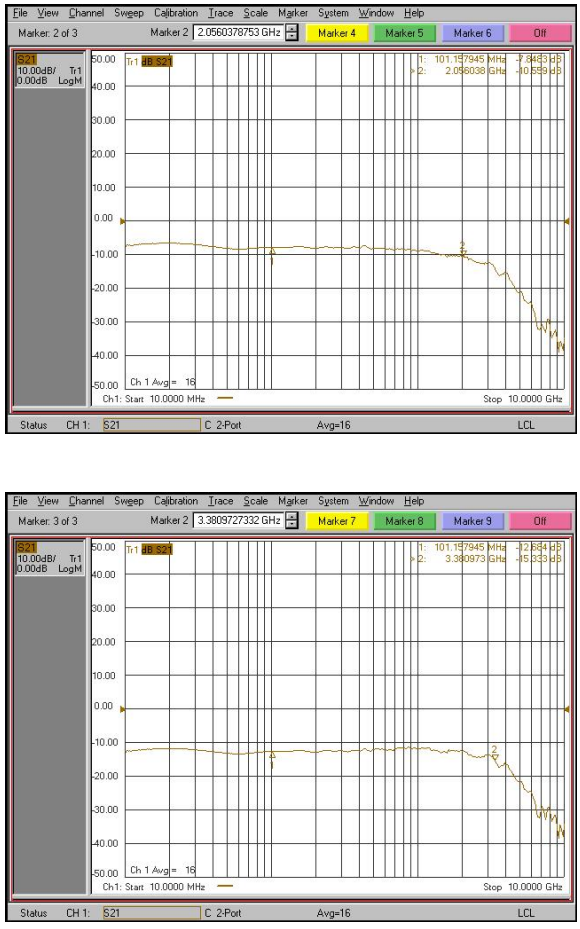


그림 8. ABC 및 AMC를 갖는 S-parameter 측정.
Fig. 8. Measured s-parameter with ABC and AMC.

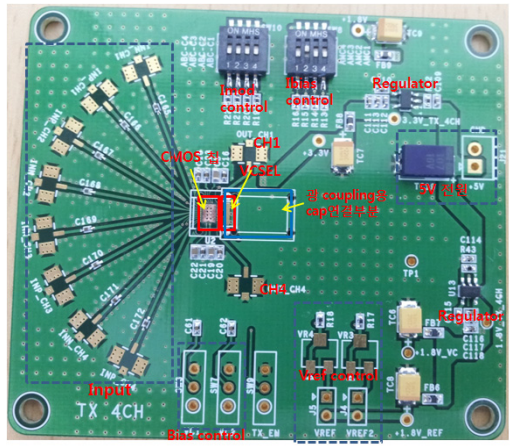
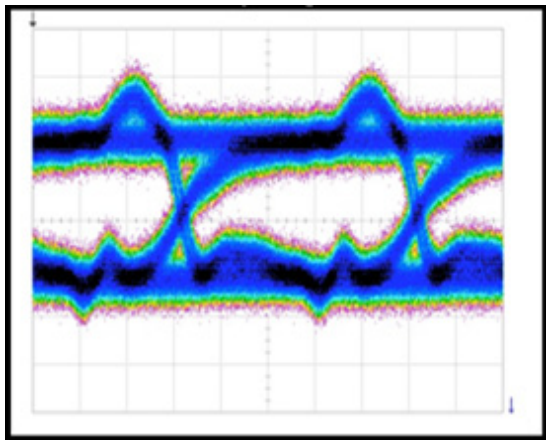


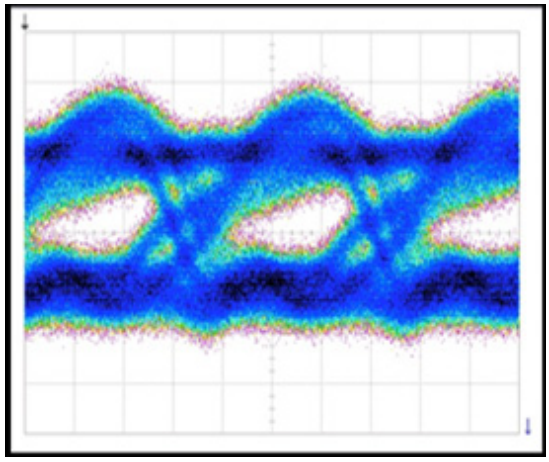
그림 9. 4채널 VCSEL Driver 테스트 보드
Fig. 9. Test Board for 4 channels VCSEL Driver.

Fig. 9 is a test board for the 4-channel VCSEL driver. It has input ports made with eight SMB connectors. The input is connected with the VCSEL through the CMOS chip for the SMB and optical measurement, being coupled with the optical fiber. The DC offers a reference current to each block using the BGR and bias block. In addition, there is a switch block for the bias that can control the reference current value. The top part shows the blocks for Imod and Ibias, each with four switches.

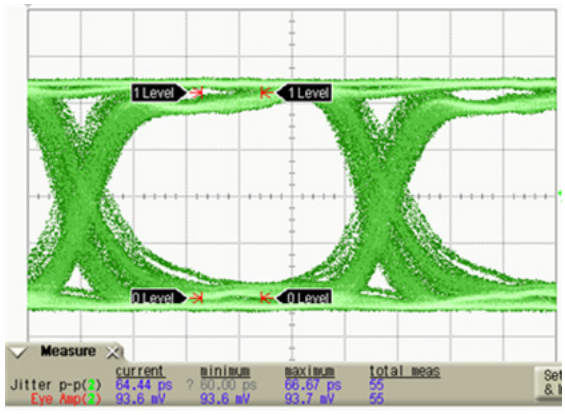
Fig. 10 shows the results of optical signal outputs when we run the VCSEL with input signals of 1.0 Gbps and 2.5 Gbps respectively. In the electrical measurement, a wide bandwidth was produced, and therefore it seemed that the operation at 2.5 Gbps would have no problem. However, when we measured through the optical fiber after connecting the VCSEL, the operation at 2.5 Gbps appeared unstable. It was determined from a simulation with a VCSEL equivalent circuit that the performance is deteriorated by the parasitic capacitors and other factors. In Figure 10(a), the size of the signals are the same, but as the data rate increases, the eye openings are reduced. That is, the bandwidth is reduced. In Figure 10 (b), the output swing is small. That is, the output voltage of the VCSEL is 2.1 V, but as it is higher than the design value of 1.6 V, the range of the output swing is reduced. Figure 10(c) shows the performance after solving the above problems. It also shows the measurement results at 2.5 Gbps for 50mV, and eye diagrams under the conditions of PRBS 2^{-7}-1 at 1.8V, and Vbias of 0.68 mV. The approved bias and modulation currents area 50 uA reference current. Using this current, 100 uA and 200 uA can both be increased by two-and four-times the original value. To reduce the current consumption, we set the reference current with the minimum value (50uA). To increase the size of the voltage output, rather than blindly increasing the current, the output impedance should also be expanded at the same time. In addition, for the DC bias, a point to increase the output swing also should be determined. Thus, by continuously tuning various values, the range of output swing should be increased.



(a) 1.0 Gbps Signal



(b) 2.5 Gbps signal



(c) 3.5 Gbps signal

그림 10. 데이터 속도에 관한 아이 패턴 시뮬레이션 결과: (a) 1.0 Gbps,(b) 2.5 Gbps and (c) 3.5 Gbps 신호
Fig. 10. Simulated Eye Patterns with respect to the Data Rates: (a) 1.0 Gbps, (b) 2.5 Gbps and (c) 3.5 Gbps signal.

The performance of the proposed VCSEL driver is summarized in Table 2. The proposed optical power control loop properly operates with respect to the variation of the incident average and modulated optical power into monitoring photo diode (MPD). ABC and AMC loop can control the bias and modulation current of the optical transmitter by the step of 0.5 rnA and the total range of 7.5 rnA. The whole chip consumes 36 mA per channel of DC currents at a single 1.8V supply under the maximum bias (0.5 ~ 7.5 rnA,▽7 mA) and modulation (2 ~ 7.5 rnA, ▽5 mA) currents[6].

표 2. 4채널 VCSEL driver 성능 요약
Table 2. Performance Summary of the 4 channel VCSEL driver.

Parameter	Target	Results
Bandwidth (−3dB)	2.5 GHz	2.5 GHz
Data Rate	2.5 Gbps	2.5 Gbps
DC Current Consumption	< 40 mA	19 mA
Output Impedance	50 Ω	50 Ω
Power Supply	Core 1.8V, I/O 3.3V	Core 1.8V, I/O 3.3V
Path Gain	> 3 dB	4 dB
Technology	0.18 μm CMOS	0.18 μm CMOS
Ibias Range	5~20 mA	0.5~7.5 mA
Imod Raange	5~20 mA	2~7.5 mA

Ⅳ. CONCLUSION

In this paper, the design and layout of a 2.5 Gbps arrayed VCSEL driver using 0.18 μm CMOS process technology for optical transceiver having arrayed multi-channel of integrating module is confirmed. Active feedback amplifier with negative capacitance compensation is exploited. We report a distinct improvement in bandwidth, voltage gain and operation stability at 2.5Gbps data rate in comparison with existing topology. A 4 channel 2.5 Gbps VCSEL driver with the proposed adaptive optical power control is designed and implemented in 0.18 μm CMOS process technology. It has a dual power supply 1.8Vdc and 3.3 Vdc laser driver for EPON, GPON, and WPON applications with data rates up to 2.5 Gbps. In the circuit level, to enhance the

bandwidth of the pre driver, active feedback amplifier with negative capacitive compensation is proposed. Proposed 0.18 μm CMOS 2.5Gbps VCSEL driver is expected to compensate temperature effects of the VCSEL using analog AMC/APC and provides cost-effective solution such as low power, simple design for WPON and short haul multi-channel applications. The 4-CH chip consumes only 140 mW of DC power at a single 1.8V supply under the maximum modulation and bias currents, and occupies the die area of 850 μm × 1,690 μm excluding bonding pads.

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