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論 文

A Data Communication Method for Real-Time Control Systems

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實時間制御시스템을 위한 데이터通信方式

正會員 張 太 戊*

要 約 多數의 마이크로프로세서와 이를 연결해 주는 미니컴퓨터로 構成된 實時間 온라인制御시스템에서의 데이터通信의 제반양식 및 그 접속단의 한 방안이 제시되고 설계되었다. 접속단은 DMA方式으로 함으로써 방대한 制御프로그램을 단순화 할 수 있었다. 이 方式은 실제로 서울市의 交通管制시스템에서 活用되어 成功的으로 실험되었다.

ABSTRACT A data communication protocol and interface between a minicomputer and remote microprocessor-based real-time controllers are proposed and designed. Practically this method was implemented on a real-time data acquisition and on-line control system with a good performance.

1. Introduction

In many applications requiring reliable, real-time control systems, mechanical techniques are used to implement the various control fuctions. While such systems are indeed reliable and fairly well understood, they tend to bulky, complex, and expensive. In addition, they have very little flexibility beyond the basic functions for which they were designed. Thus, low-cost microprocessors are an alternative to real-time controller design.

The same thing can be told of traffic controllers. Additionally, to enhance the performance of the traffic control system, the coordination among these controllers is required. This paper proposes a data communication method adequate for this control system. The overall system can be called as a real-time data aquisition and on-line control system, which is configured in figure 1.

The central computer transmits control informations to all the intersections through multidropped telephone lines according to its console inputs and analyzed loop detectors data. Intersection controlers receive control informations from the central processor and retransmit their status and accumulated loop detectors data on the fixed timing basis. The interface between the central system and communication facilities utilizes the channel I/O method of Eclipse system for the purpose of enhancing the system transmission and receiving speed and reducing the overhead of program works. The command used to setup the data channel transfer are assembled in an accumulator and are transferred to the interface controller under direct program controls. The block of data is then automatically transferred directly between main memory and the interface controller via the data channel. Hence the control program can proceed with other tasks while the block transfer is taking place.

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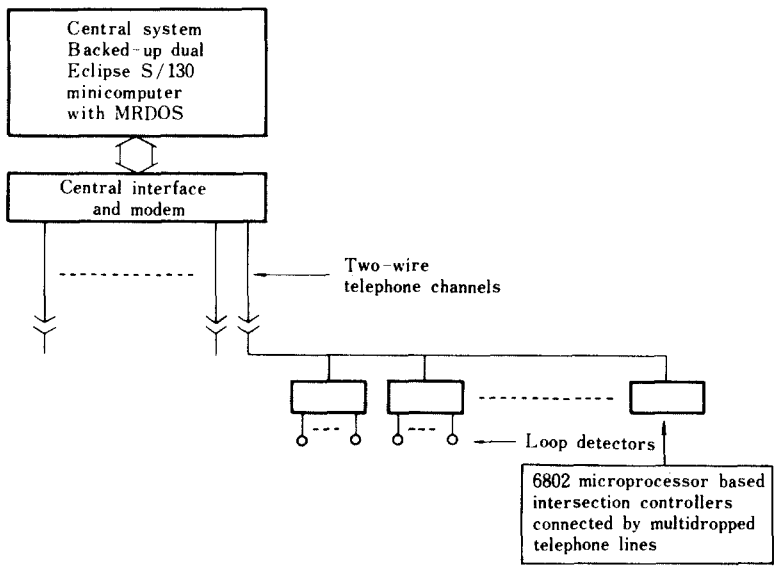


Fig. 1 Overall system configuration.

2. Theory of communication operations

Communication equipments used in this system provide the capability to exchange data with up to 16 intersections on a given channel for the purpose of reducing line costs using TDM (Time Division Multiplexing), in a one second interval. The TDM method is illustrated by the diagram in Fig. 2. The basic principles involve the alloting of time intervals for each control signal desired. With a TDM transmitter and a TDM receiver, the two-wire line is usable if audio frequencies are used. The input information is scanned, once each second, and the control signals present are transmitted to the TDM receiver. Not shown in Fig. 2 is the reverse path of transmit-receive, using the same principles. The mode of data transmission is frequency shift keying (FSK, mark: 2200 Hz, space: 1200 Hz). For a transmission to a given intersection, there are four bits of address and twelve bits of data contained in the sixteen bits of information, which is well suited for minicomputers' data processings. For a error control purpose, the transmitted data is sent twice before the intersections are expected to reply. Sixteen intersections are contacted in a one second interval, over 3000-graded leased telephone lines. Each intersection receiver has an address for comparison to the transmitted value sent by the central computer. In response to receiving the correct address, the intersection transmitter sends 16 bits of information back to the central computer. The central office receiver latches the data received and notifies the minicomputer that a word of information has been received and is ready for the minicomputer to retrieve it.

The transmission speed of the modem is 1800 bps. Both the central office and intersection units have timers, which time between valid transmissions to intersections and the reply from the intersections. If the twice transmitted data are not the same or data are not available within three seconds at the intersection site, the error signal is transmitted to the central office unit. Hence error controls can be performed by the minicomputer con-

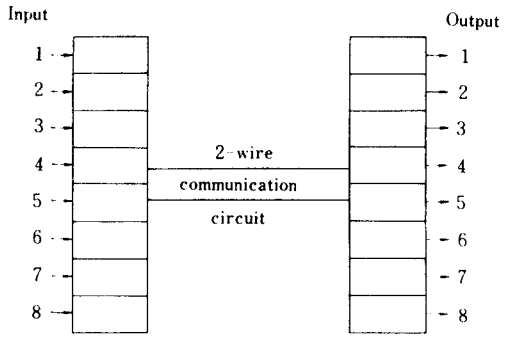
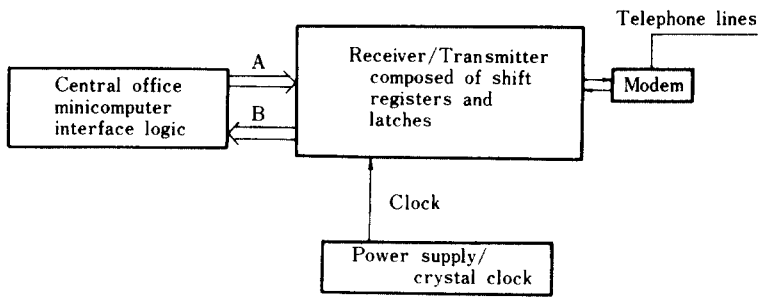


Fig. 2 TDM example.

trol software. The functional block diagram of the central communication office unit and the interfacing signals are shown in Fig. 3.

3. Interface hardware

The hardware interfacing could be easily constructed with Data General corp. vendored interface hardwares and some additional logics. The 4040 general purpose interface boards comprising normal Busy/Done flags and interrupt networks are used together with 4041 data register option, 4042 data channel connecting option, and 4044 extended wire-wrap pins and sockets. Data channel operation is not so different from normal cycle-stealing con-



A; 16 bits bus (4 bits address 12 bits data)
Channel Enable (1-8)····Minicomputer I/O interface logic decodes the computer address computer address and enables the proper channel.
Data Outstrobe····Enables 8 chnnnels at once.
Indicates time that enabled channel should latch the incoming data in the in the data-in bus.
Data Instrobe····Enables 8 channels at once.
Indicates time that received and stored data should be placed on the output bus.
B; 16 bits data bus
Received Data Ready (1-8)····8 lines, one per channel Notifies minicomputer interface logic that 16 bits of data have been received and latched from the intersection.
Ready to load.
Received Error Flag (1-8)····8 lines, one per channel Notifies minicomputer interface logic that an intersection reply is invalid.

Fig. 3 Central communication interface block diagram.

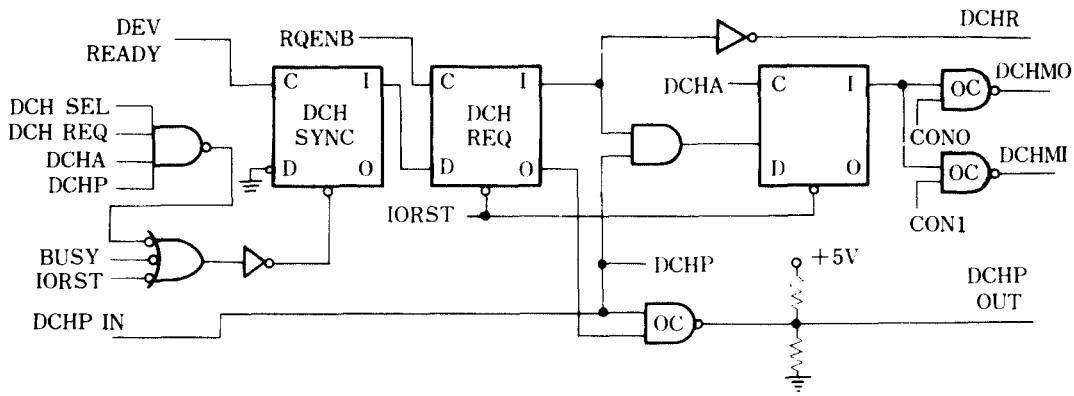
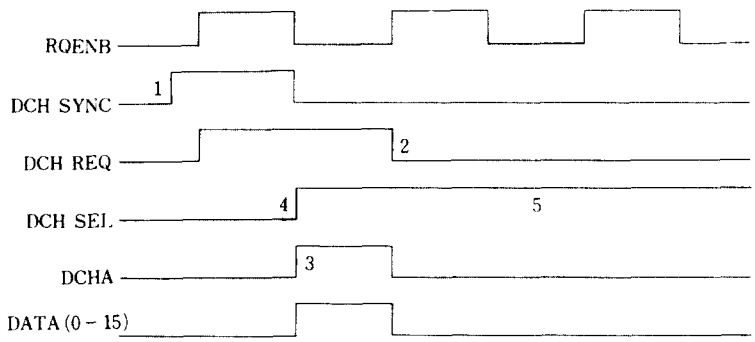


Fig. 4－1 Data channel control network.



comments;

1. DCH SYNC set by device upon completion of operation
2. DCH REQ remains asserted to obtain back-to-back transfer
3. DCH SYNC cleared by DCHA of processor data channel response
4. DCH SEL set if DCH REQ and DCHP IN are asserted, otherwise cleared
5. Interface asserts transfer mode DCHMO, DCHM1 when DCH SEL is set

Fig. 4－2 Data channel acknowledge sequence.

cept as shown in Fig. 4. Two registers, the word counter and memory address counter, are included in this option card. The detailed operations and digital networks are not introduced, which are well illustrated in reference manuals.

4. Control program

The control program runs under Data General corp. vendored MRDOS (Mapped Real-time Disk Operating System) operating system. The control program is fully interactive to meet a real-time control systems' requirement. Direct memory access initiating routine is the highest priority task in multi-task environment control program, envoked every second by a user defined clock of MRDOS.

The output and input portion of this routine is as follows.

```
OUTPUT
    LDA    0, CWDO   ; output command word
    LDA    1, NCH    ; number of channels
    NEG    1, 1
    INC    1, 1
    LDA    2, OUTP   ; address of output table
    DOC    0, DMA    ; DMA = DMA device code
    DOAP   1, DMA    ; clear
    DOBS   2, DMA    ; start DMA
  CWDO:    1B12+1B15
INPUT
    LDA    0, CWDI   ; input command word
    LDA    1, NCH
    NEG    1, 1
    INC    1, 1
    LDA    2, LADDR  ; logical address of DMA
                       table in buffer
    DOC    0, DMA
    DOAP   1, DMA
    DOBS   2, DMA
  CWDI:    1B12+1B14
```

5. Conclusion

A useful method of interfacing between a minicomputer and remote microprocessor-based controllers is proposed and implemented. Some of good characteristics of this interfacing are as follows:

(1) Fast responsiveness

This characteristic, which is the first requirement of real time control systems, can be achieved. All the functioning statuses of remote controllers can be transferred to the central site within one second, which envoke the central processor to do adequate controls. The direct memory access I/O method contributes much to this characteristic.

(2) Reliability

This system provides backed-up dual central computer and some error control strategies described in section 2 of this paper to achieve this goal. Even if the communication fails, microprocessors of the local controllers has the local intelligence and can perform the off line control without coordinations.

(3) Flexibility

By changing the format of 16 bits information to be sent and received and modifying the central control program, users can easily append useful additional functions to the system.

(4) Cost saving

Multidropping method can contribute to the line cost saving. But driving power requirements limit the number of intersection controllers up to 8 or 9 for stable operation.

(5) Heterogeneity

Though the user adopts different kinds of intersection controllers, the interface works well if the information length (16 bits) is compatible.

(6) Extensibility

More intersection controllers can be included in the system by a slight change in the contal program parameters and the number of communication channels without degrading the control program performance.

This method of data communication was adopted in Seoul Computerized Traffic Control system. But this method can be applied to other real-time control systems where one second is the sufficient interval for time critical events. According to the city police reports, the traffic control system gives about 30% reduction in stop numbers of traveling vehecles, and also 30% increase in the average traveling speed of vehecles in the computerized area.

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