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비트 패턴드 미디어 기록장치를 위한 LLR 컨트롤러

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Log-Likelihood Ratio Controller for Bit-Patterned Media Recording

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요 약

비트 패턴드 미디어 기록장치는 기록밀도를 제곱 인치당 1 테라비트 이상을 달성할 수 있기 때문에 차세대 자기 저장장치로 주목받고 있다. 기록밀도를 증가시키기 위해서는 하나의 비트를 저장하는 아일랜드들의 간격이 줄어들어야 하는데 이는 인접 심볼간 간섭과 인접 트랙간 간섭을 증가시킨다. 본 논문에서는 비트 패턴드 미디어 기록장치를 위한 패리티 체크 행렬을 활용한 LLR 컨트롤러 방식은 제안한다. LLR 컨트롤러는 LDPC 부호의 신드롬과 패리티 체크 부호를 활용하여 LDPC 디코더의 출력값을 변형한다. 제안하는 LLR 컨트롤러를 활용한 반복적 LDPC 디코딩 방식은 LDPC 부호만 사용했을 때, LLR 컨트롤러를 사용하지 않고 반복적 LDPC 디코딩 방식을 사용하였을 때보다 우수한 성능을 보여준다.

키워드 : 비트 패턴드 미디어 기록장치, 데이터 저장장치, 반복적 디코딩, 로그 우도비, 저밀도 패리티 체크 부호

Key Words : Bit-patterned media recording, data storage system, iterative decoding, log-likelihood ratio, low-density parity check code.

ABSTRACT

Bit-patterned media recording (BPMR) is a possible future magnetic recording system with potential to extend areal density (AD) beyond 1 terabit per square inch. To achieve high AD, gaps between the islands that store bits of data must be reduced; however, this introduces significant issues such as intersymbol and intertrack interference. In this paper, an effective decoding scheme using a low-density parity check (LDPC) code, with a log-likelihood ratio (LLR) controller to improve bit error rate (BER) performance, has been introduced. The LLR controller modifies the LLR output of the LDPC decoder using coefficients obtained through the relationship between the syndrome and the parity check matrix. The syndrome is in fact not only a set of symptoms indicating errors but also indicates which parity check constraints (equations) have not been satisfied by the received codeword. Considering this property with the parity check matrix, the LLR controller generates an efficient coefficient and modifies the LDPC decoder LLR output. Using computer simulation, we have shown that the BER performance of this iterative LDPC decoding scheme, with the LLR controller, is superior to that of both the LDPC alone and the iterative LDPC decoding scheme without the LLR controller.

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Ⅰ. Introduction

Current hard disk drives (HDD), with perpendicular magnetic recording technology, are faced with the superparamagnetic problem, which hinders increasing the areal density (AD) beyond 1 terabit per square inch (Tb/in^2). This has led to the invention of new magnetic recording technologies, including bit-patterned media recording (BPMR)[1],[2], two-dimensional magnetic recording[3], heat-assisted magnetic recording[4], microwave-assisted magnetic recording[5] and so on, in attempts to overcome these problems and increase the AD. BPMR has been extensively studied and is thought of as a future technology for next generation magnetic storage systems. In a conventional magnetic storage system on granular media, an ensemble of grains store one data bit. In contrast, in a BPMR system, each island stores one data bit recorded on bit-patterned media (BPM), which comprises lithographically patterned, isolated magnetic islands[6]. BPM is able to decrease both transition and track edge noise, and also provides the advantages of decreased nonlinear bit shift, easier tracking, and good thermal stability[1],[7]. In terms of signal processing and error control coding (ECC), BPMR has met some difficulties. Decreasing the interval between islands is needed, in down- and cross-track directions, to achieve high AD in BPMR, however new problems, such as intersymbol interference (ISI) and intertrack interference (ITI), i.e., 2-D ISI, seem to be unavoidably[8],[9]. To address this, partial response maximum likelihood (PRML), applied to a system where the channel response is equalized to a partial response (PR) pulse shape and maximum likelihood (ML) sequence detector, has been employed, to help detect the input data[10]. Also, since the track misregistration (TMR) that is generated when the recording heads cannot remain at the center of the main data track degrades system performance, techniques have been proposed for estimating TMR from the readback signals, to alleviate the TMR effect[11-13]. In addition, in order to improve BPMR system performance, researchers have investigated many signal processing techniques, including signal detections, ECCs, and modulation codes, for BPMR systems[14-19].

Strict requirements—for a low probability of decoding failure and for a high code rate—are placed on data storage systems (HDD, solid state drives, and optical storage systems). Since data storage systems cannot retransmit data—unlike typical communication systems with retransmission mechanisms, such as automatic repeat requests (ARQ)—the error floor for low-density parity check (LDPC) code should be $< 10^{-12}$ in word (sector) error rate[20].

In this paper, we propose an effective decoding scheme, using an LDPC code having a log-likelihood ratio (LLR) controller to improve bit error rate (BER) performance. The LLR controller scheme exploits the syndrome property, which is not only a set of symptoms that indicate errors, but also indicates which parity check constraints have not been satisfied by the received codeword. Considering this property with a parity check matrix, the LLR controller generates an efficient coefficient, and modifies the LDPC decoder LLR output.

The rest of this paper is organized as follows. In Section II, LDPC code is briefly introduced, and the LLR controller is described in detail. In Section III, the BPMR channel model and PRML detection have been presented, Section IV provides simulation and results, and conclusions are presented in Section V.

Ⅱ. Iterative LDPC Codes with the Proposed LLR Controller Scheme

2.1 LDPC codes

Binary LDPC codes were first introduced by Gallager in the early 1960s, and are binary linear block codes defined by designing a sparse parity check matrix **H**, that has (n - k) rows and n columns[21]. LDPC codes were not used for 30 years, due to the complexity of iterative decoding algorithm, before being rediscovered by Mackay and Neal[22]. Each row vector of the k x n generator matrix **G,** that encodes **u** of a length k vector for the user data into **c** of a length n vector for the codeword, and each row vector of the parity check

matrix **H,** is orthogonal. Therefore, the parity check matrix **H** satisfies $\mathbf{GH}^T=\mathbf{0}$, and then $\mathbf{cH}^T=(\mathbf{uG})\mathbf{H}^T=\mathbf{S}=\mathbf{0}$ where ***S*** is a syndrome.

An LDPC code can be expressed by a bipartite graph (Tanner graph) representing parity check equation as shown Fig. 1. A bipartite graph consists of variable and check nodes and links variable and check nodes. Each variable node matches a bit in the codeword, and each check node expresses a parity check equation (i.e., a row in the parity check matrix **H**). An edge between the variable and check node exists if and only if the bit participates in the parity check equation represented by the check node. A sum–product algorithm (SPA) is an iterative decoding, based on the maximum a posteriori algorithm[23]. After setting the initial SPA value—which depends on the channel characteristics—the information is interchanged between the variable and check nodes. If $\mathbf{cH}^T=\mathbf{0}$ at each iteration, or the number of iterations equals the maximum limit, the iterative decoding process stops.

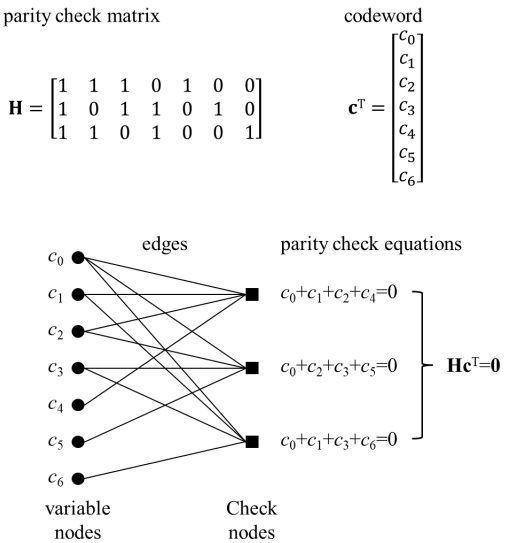

그림 1. 패리티 체크 행렬과 이분 그래프상의 변수 노드와 체크 노드
Fig. 1. A parity check matrix and bipartite graph linking variable and check nodes.

2.2 The proposed LLR controller scheme

For a retransmission system such as ARQ, a stopping criterion for LDPC codes using the syndrome weight (or the number of satisfied parity check constraints) was proposed, to predict LDPC decoding failure[24]. Since LDPC decoding often fails in the low signal to noise ratio (SNR) region, the decoding algorithm continues until the number of iterations equals the maximum limit—and the decoding complexity is increased as well. To avoid unnecessary iterations and complexity, the syndrome is used as the proposed stopping criteria.

In our research, the proposed LLR controller calculates appropriate coefficients, and modifies the LLR output of the LDPC decoder by exploiting the syndrome property. Algorithm 1 briefly summarizes the proposed LLR scheme. After the LLR output of the LDPC decoder $L(\mathbf{u})$ is converted to a hard decision vector **a**, the syndrome **S** is calculated by multiplication of the hard decision vector **a** and parity check matrix $\mathbf{H}^T$, as follows:

$$\mathbf{S}=\mathbf{a}\cdot\mathbf{H}^T. \tag{1}$$

알고리즘 1. 제안하는 LLR 컨트롤러의 알고리즘
Algorithm 1. Proposed LLR controller algorithm.

```
Input: L(c) and L(u)
for i =0 to N-1 do
  if L(ui)<0 then
    ai=1.
  else
    ai=0.
  end if
end for
Calculate syndrome S by aH^T.
if S = 0 then
  for i =0 to N-1 do
    Calculate Le(ui) = L(ui)- L(ci).
  end for
else
  for i =0 to N-1 do
    if dH(hi, S) = 0 then
      Decide that i-th position is in error.
      for j =0 to N-1 do
        Calculate Le(ui) = L(ui)- L(cj).
      end for
      Stop LLR controller.
    else
      Calculate β = dH(hi, S) / w(S).
      Calculate Le(ui)=α·β·L(ui)- L(ci).
    end if
  end for
end if
```

If **S** is **0** (zero vector or all zeroes), **a** is a valid codeword. So, extrinsic information $L_e(u_i)$ can be expressed as:

$$L_e(u_i) = L(u_i) - L(c_i). \quad (2)$$

However, if **S** is not a zero vector, the codeword has either a one bit error or multiple bit errors. When a one bit error in the codeword occurs, **S** is the column of **H** corresponding to the location in error. In other words, **S** is equal to the i-th column vector $\mathbf{h}_i$ of **H**, and the Hamming distance between $\mathbf{h}_i$ and **S** (i.e., $d_H(\mathbf{h}_i, \mathbf{S})$) is zero. After the error in the i-th location is corrected, extrinsic information $L_e(u_i)$ is calculated using equation (2). When multiple bit errors in a codeword occur, however, coefficient β_i of the i-th position is calculated by dividing the Hamming distance $d_H(\mathbf{h}_i,\mathbf{S})$ by the weight of the syndrome $w(\boldsymbol{S})$, as follows:

$$\beta_i = \mathrm{d}_{\mathrm{H}}\left(\mathbf{h}_{\mathrm{i}}, \mathbf{S}\right) / w\left(\mathbf{S}\right) \quad (3)$$

This means that the coefficient is decreased in the place where the probability of error is high, and is increased in the place where the probability of the error is low. Lastly, extrinsic information $L_e(\mathbf{u})$ is calculated as shown in (4) where α is a weighting factor.

$$L_e(u_i) = \alpha \cdot \beta_i \cdot L(u_i) - L(c_i). \quad (4)$$

Fig. 2 presents an example of the LLR controller with parity check matrix with a row weight of 4 and a column weight of 3[21]. For example, after the LLR output of the LDPC decoder $L(\mathbf{u})$ is converted to a hard decision vector **a** = {1, 0, 0, 0, ⋯, 1, 0, 0, 0} as shown in Fig. 2, **S** is calculated by multiplication of the **a** and $\mathbf{H}^{\mathrm{T}}$, as in (2). However, since $d_H(\mathbf{h}_i, \mathbf{S})$ for all i is not zero, β_0 of 0.5 is calculated by dividing $d_H(\mathbf{h}_0, \mathbf{S})$, of 3, by syndrome weight $w(\boldsymbol{S})$, of 6. Fig. 3 shows BER performance according to a weighting factor α, to improve system performance when SNR is 8 dB. From the figure, since BER performance is best when α is 3 or 3.5, α is set to 3.

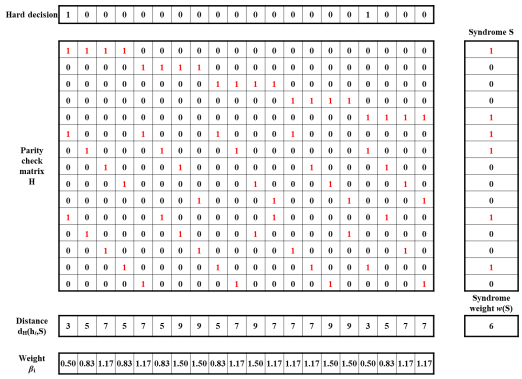

그림 2. 행 무게가 4이고 열 무게가 3인 패리티 체크 행렬을 사용한 LLR 컨트롤러의 예제
Fig. 2. An example of the LLR controller with a parity check matrix with a row weight of 4 and column weight of 3.

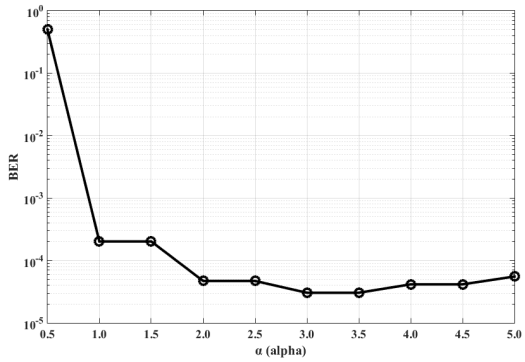

그림 3. SNR이 8dB에서 가중치 α에 따른 BER 성능
Fig. 3. BER performance according to a weighting factor α when SNR is 8 dB.

Ⅲ. BPMR Channel Model and PRML Detection

3.1 BPMR channel model

In a BPMR system, a BPM layout can be arranged on a regular array, as shown Fig. 4. L_x, L_z, T_x and T_z are the down-track direction island length, cross-track direction island length, the bit period, and track pitch, respectively. In a regular-array BPM layout, the island on the main track is mainly affected by the ITI effect from the two islands along the upper and lower track, respectively, which are located immediately adjacent to the island on the

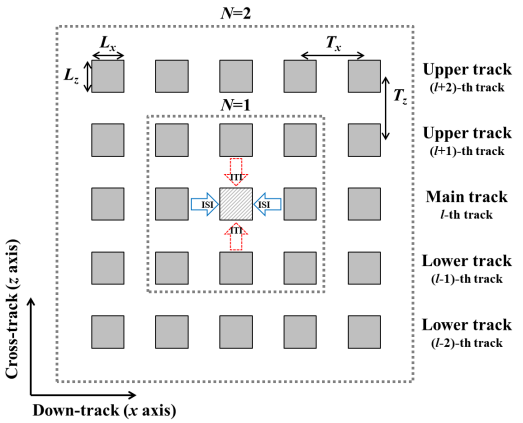

그림 4. BPM 레이아웃의 구조 및 주변 아일랜드로부터 받는 영향의 길이 예제
Fig. 4. Structure of the BPM layout, and examples of the interference length from neighboring islands.

main track. In addition, the island on the main track is mainly affected by ISI effects from the left and right islands on the main track, respectively.

Fig. 5 illustrates a block diagram of the proposed system. Before passing through the BPMR channel, the binary data $c_{p,q} \in \{0, 1\}$ is magnetized into $d_{p,q} \in \{-1, +1\}$ (recorded bits). For recorded bits, the 2-D Gaussian island pulse response $P(z, x)$ in a BPMR medium can be defined as follows[25,26]:

$$P(z,x) = A\exp\left\{-\frac{1}{2k^2}\left[\left(\frac{z}{\mathrm{PW}_z}\right)^2+\left(\frac{x}{\mathrm{PW}_x}\right)^2\right]\right\}, \tag{5}$$

where A is the normalized peak amplitude, and z and x are the indices in the cross- and down-track directions, respectively; k is 1/2.3548 (constant) represented by the relationship between the standard deviation of a Gaussian function and PW50, which is a parameter of the pulse width at half of the peak amplitude; PW_z and PW_x are the PW50 of the cross- and down-track pulse, respectively. In our study, we used A=1. The 2-D channel response coefficients $h(m, n)$, which are obtained by sampling the 2D Gaussian island pulse response, can be expressed as:

$$h(m,\ n) = P(mT_z, nT_x), \tag{6}$$

where $P(z, x)$ is the 2-D Gaussian island pulse response, and m and n denote the indices of bit islands for cross- and down-track directions, respectively. The readback signal (received signal) $r_{p,q}$, corrupted by electronic noise, can be written as follows:

$$\begin{aligned} r_{p,q} &= d_{p,q} \otimes h(m,n) + n_{p,q} \\ &= \sum_{m=-N}^{N}\sum_{n=-N}^{N} c_{p-m,q-n}\cdot h(m,n) + n_{p,q}, \end{aligned} \tag{7}$$

where signal $r_{p,q}$ is the readback signal on the q-th data bit along the p-th track; $\otimes$ is the 2-D convolution operator; $n_{p,q}$ is electronic noise modeled as an additive white Gaussian noise, with zero mean and variance σ^2; and N is the length of the interference from neighboring islands in the rectangular array illustrated in Fig. 4. In our study, since the interference from the islands in N = 2 is almost zero, we assume for simplicity that N = 1.

3.2 PRML detection

In conventional data storage systems, since ISI is equalized to a target response, PRML is exploited to combat ISI[27], and the equalizer output is decoded by the channel decoder. A PR equalizer handles a readback signal as a PR pulse shape, and when the PR pulse shape does not exactly correspond with the recording channel, the equalizer output has an inaccurate value, due to noise enhancement. After the input data $d_{p,q}$ from the q-th data bit along the p-th track has passed through the BPMR channel, the readback signal $r_{p,q}$ is input to each equalizer. The equalizer output $e_{p,q}$ is calculated using

$$e_{p,q} = r_{p,q} \otimes u_{m,n} = \sum_{m=0}^{L_m-1}\sum_{n=0}^{L_n-1} r_{p-\lfloor L_m/2\rfloor+m,\,q-\lfloor L_n/2\rfloor+n}\cdot c_{m,n}. \tag{8}$$

In (8), $u_{m,n}$, L_m, and L_n are equalizer coefficient, equalizer length for cross-track direction, and equalizer length for down-track direction, respectively. We used a 5 × 5, 2-D equalizer. i.e., L_m= L_n= 5. The equalizer coefficients are updated using a least mean square algorithm, as shown in (9):

$$c_{m,n}^{(k+1)} = c_{m,n}^{k} + \mu\left(e_{p,q} - \sum_{n=-L_f}^{L_f} d_{p,q-n} \cdot f_{0,L_f+n}\right) r_{p,q}, \qquad (9)$$

where $c^{(k+1)}$and c^{k} are updated coefficient and current coefficient, respectively; μ is an adaptation gain; and f is the 1 x ($2L_f$+1) PR target coefficient. In our study, we set L_f = 1, and the PR target coefficients are (0.1, 1.0, 0.1). After the readback signal $r_{p,q}$ is processed by the equalizer, the equalizer output $e_{p,q}$ is decoded by the ML decoder, based on a Viterbi algorithm. In [28], a soft output Viterbi algorithm (SOVA) was proposed to calculate the LLR value. The equalizer output $e_{p,q}$ is input to the SOVA decoder, which output a sequence based on the corresponding PR target. The branch metric of the SOVA decoder is calculated as shown in equation (10):

$$\lambda_{p,q}(s_j, s_k) = \{e_{p,q} - (f_{0,0} \cdot \hat{a}_{p,q-1}(s_j) + f_{0,1} \cdot \hat{a}_{p,q}(s_j) + f_{0,2} \cdot a_{p,q+1}(s_k))\}^2, \qquad (10)$$

where s_j, s_k, $\hat{a}(s_j)$, and $a(s_k)$ are the current state, the next state, the decision at s_j, and the decision at s_k, respectively. A final SOVA output $L(c_{p,q})$ is then delivered to the LDPC decoder.

Ⅳ. Simulation and Results

We assume that data are read per page, and 100 pages are simulated. Each page has 4096 × 100 bits. The down-track and cross-track direction island lengths (L_x and L_z respectively) are 11 nm. The bit period T_x and track pitch T_z are 18 nm, at 2 Tb/in^2. We set PW$_x$ to 19.4 nm, and PW$_z$ to 24.8 nm, for the 2-D island pulse response. The SNR is defined as $10\log_{10}(1/\sigma^2)$. The LDPC code size is (4096, 3616), the coderate for one LDPC code is 0.88, and the number of LDPC decoder iterations is 10. The decoding algorithm used for the LDPC decoder is the standard sum‐product algorithm in the logdomain, and there are five iterations between the LDPC decoder and the LLR controller.

To evaluate the performance of the proposed LLR scheme, we compare the BER performance in the

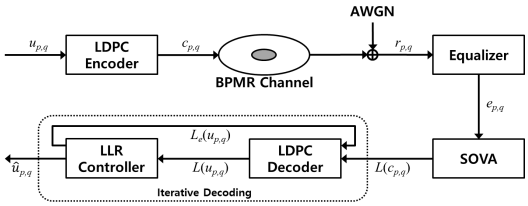

그림 5. 제안하는 시스템 모델의 블록 다이어그램
Fig. 5. Block diagram of the proposed system model.

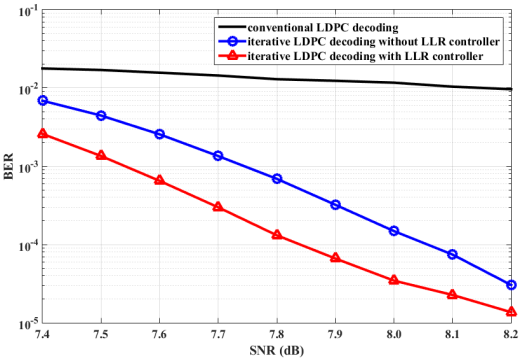

그림 6. SNR에 따른 제안하는 LLR 컨트롤러의 방식의 BER 성능
Fig. 6. BER performance of the proposed LLR controller scheme according to SNR.

LDPC code alone, iterative LDPC decoding without LLR controller, and iterative LDPC decoding with LLR controller, as shown Fig. 5.

Fig. 6 illustrates the BER performance of the proposed scheme according to SNR. When AD is 2 Tb/in^2, the proposed iterative LDPC decoding, with LLR controller, shows performance gain of ~0.2 dB, compared to the iterative LDPC decoding, without LLR controller. In addition, the performance of the iterative LDPC decoding, with LLR controller, is better than that of the conventional LDPC code.

Ⅴ. Conclusion

In this study, we proposed an iterative LDPC decoding, with LLR controller. For the ARQ system, to reduce complexity and an iteration of LDPC decoding, stopping criteria for LDPC codes using the syndrome are proposed, to predict LDPC decoding failure. Since the syndrome weight demonstrates parity check constraints, it is a good

measure for evaluating the codeword. The proposed LLR controller scheme calculated appropriate coefficients, and modified the LLR output of the LDPC decoder, by exploiting the property of the syndrome. In the results, the proposed iterative LDPC decoding, with the LLR controller scheme, performed better than that without the LLR controller.

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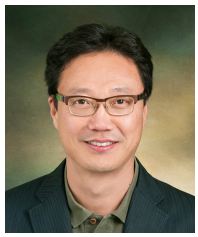

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